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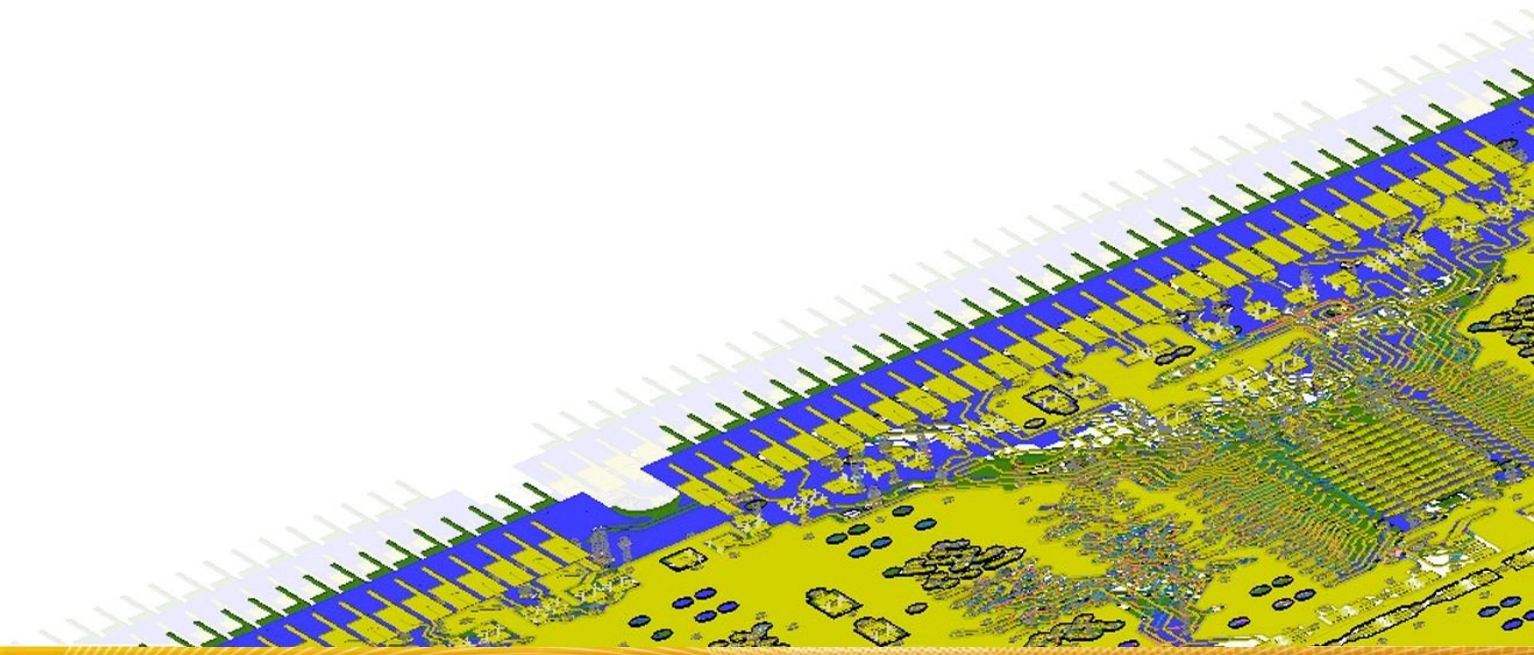
Design Space Exploration for Signal Integrity

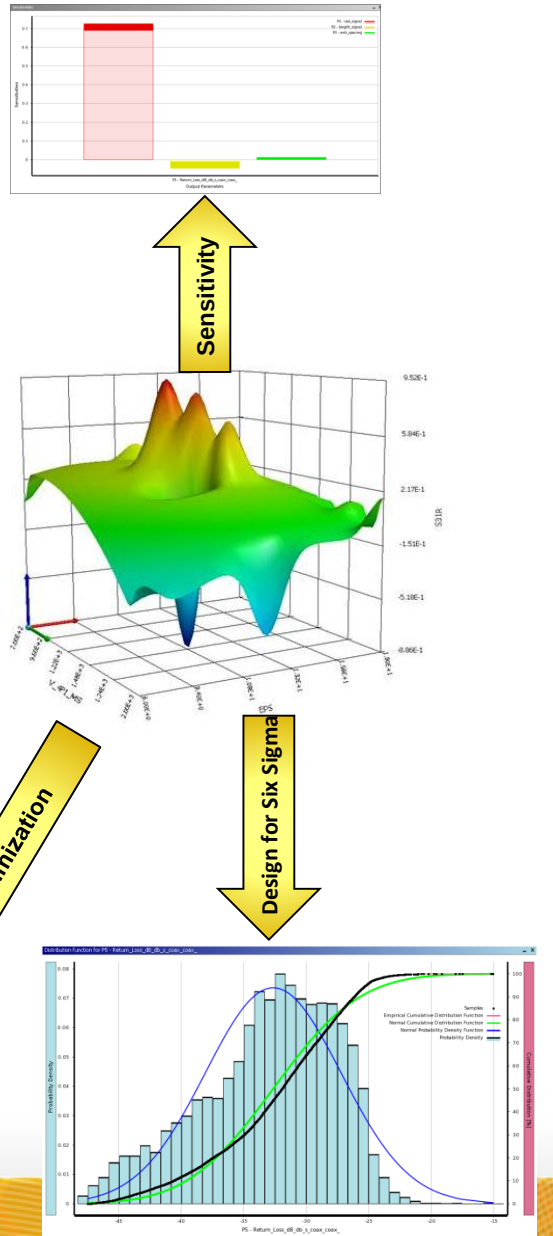


Overview

- **Introduction to Design Space Exploration**
  - **Cornerstone Technology**
  - **DesignXplorer**
- **Utilizing Design Space Exploration for Signal Integrity**
  - **Pre-layout what-if analysis**
  - **Post-layout Optimization**
  - **Manufacture variables study(6 sigma)**
- **Full Hardware Utilization for Design Space Exploration**
  - **High Performance Computing (HPC)**
  - **Distributed Solve Option (DSO)**
- **Conclusions**

Introduction to Design Space Exploration

- **Design Space Exploration is the ability for a user to explore the design space of a structure in simulation space so that they can have a design with optimum performance and manufacturability**
- **Design Space Exploration is MORE than an optimization.**
  - A simple optimization is similar to walking a foot path to a desired destination though the forest… The walker knows nothing about the surrounding area away from the path other than they 'seem' to arrived at their destination
- **Design Space Exploration is the exploration of a design's performance in the whole design space. Each variable is explored so that there can be many paths to an optimum with much more insight into the sensitivities of output quantities with respect to the design variables.**

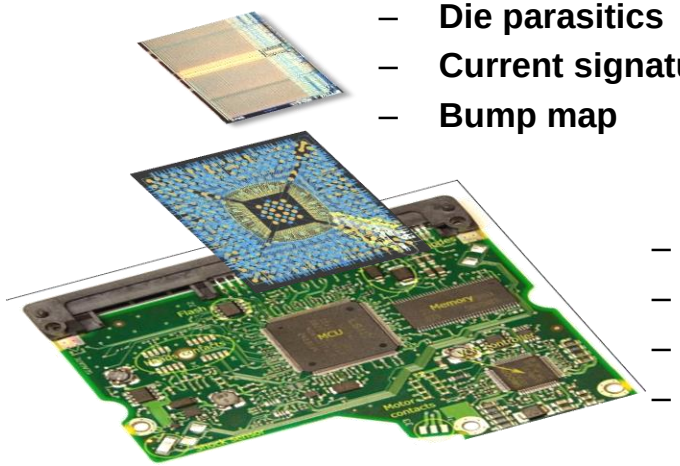


Why Using Design Space Exploration in SI?

- Electronics is hierarchy, different variable takes different role, those variables combination also displays different effect.

- Signal Integrity's goal is searching a balance design---trade off between performance and cost.

- **Chip**
  - On-chip decoupling
  - Die parasitics
  - Current signature
  - Bump map

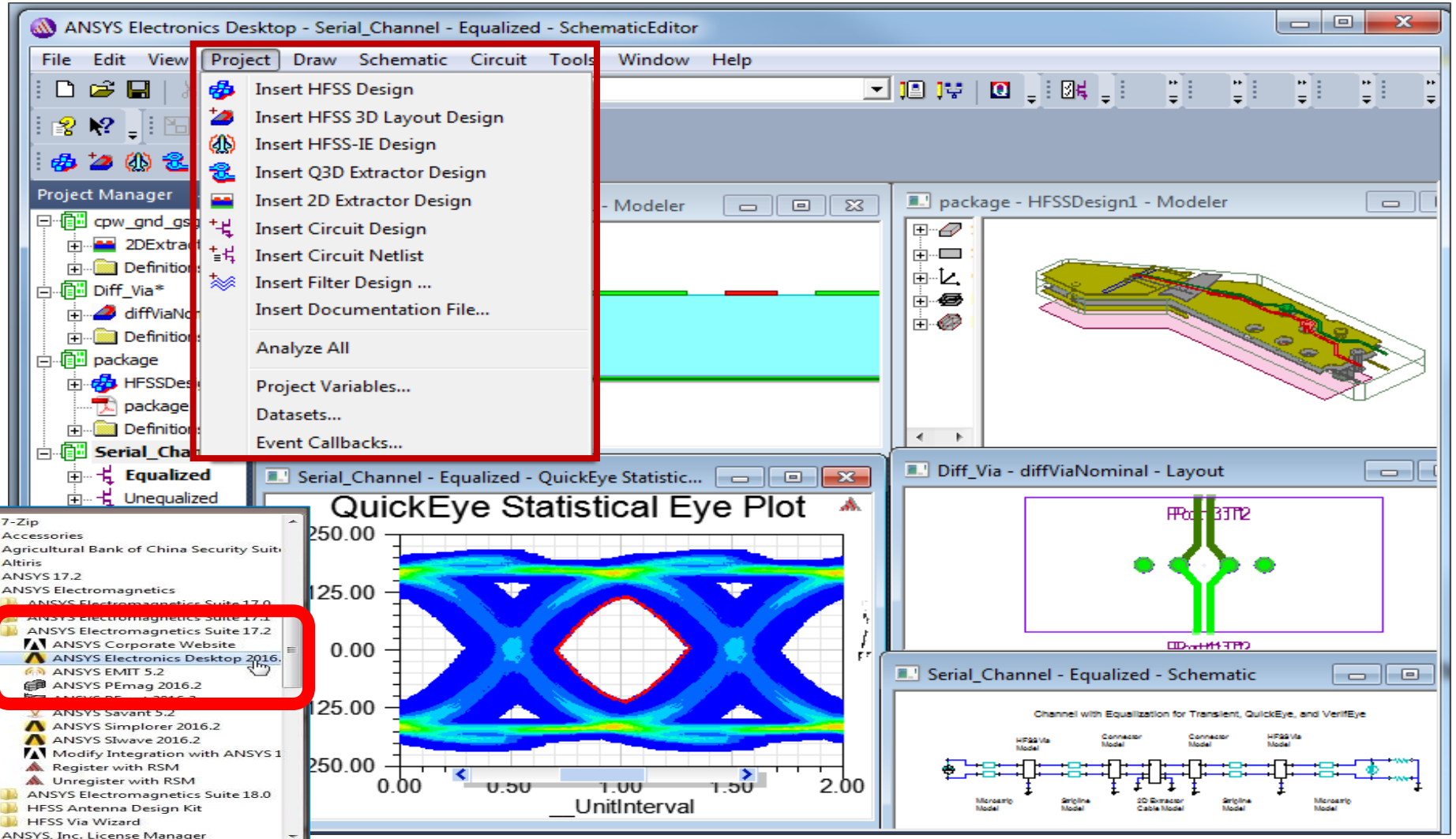


- **Package**
  - Plane shapes
  - Discretes decoupling
  - I/O routing
  - Ball map

- **PCB**
  - Channel/SSO Analysis
  - Multi-domain
  - EMI Due to Current Signature

Dr. Howard Johnson:
"Maximize the performance and minimize the cost of interconnection technology used in high-speed digital designs"
From http://www.sigcon.com

ANSYS Electronics Desktop: Integrated platform for SI



Single Desktop for:

HFSS

Q3D

HFSS 3D Layout

Planar EM

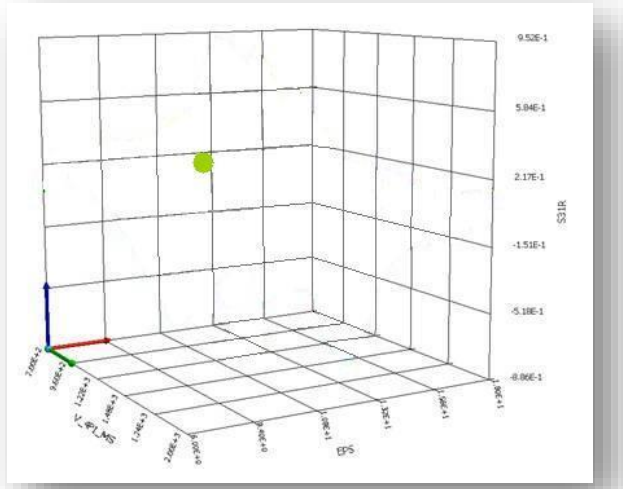
Circuit

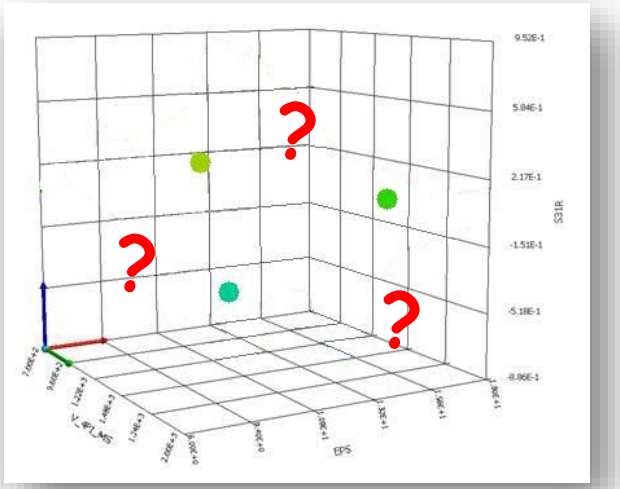
System

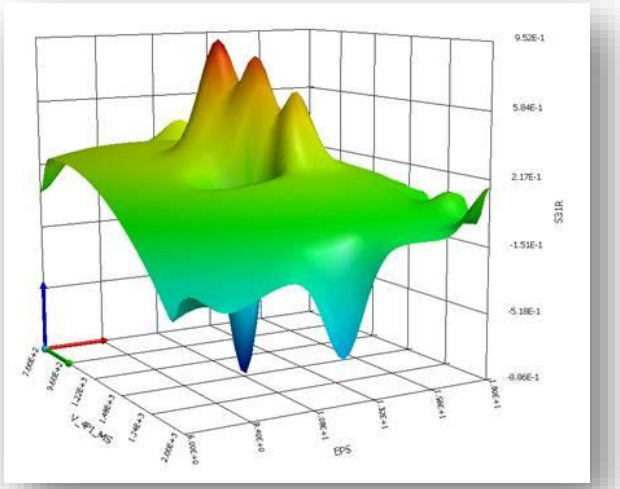
Tight integration between circuit and 3D simulation

What is DesignXplorer?

- **DesignXplorer is ANSYS powerful approach to explore, understand and optimize your engineering challenges for ANSYS Multiphysics analysis solvers, including electromagnetic.**
  - Determine the key parameters influencing the design
  - Explore and understand the performance at other design or operating conditions
  - Find the conditions which give the best performance
  - Explore the robustness of the design

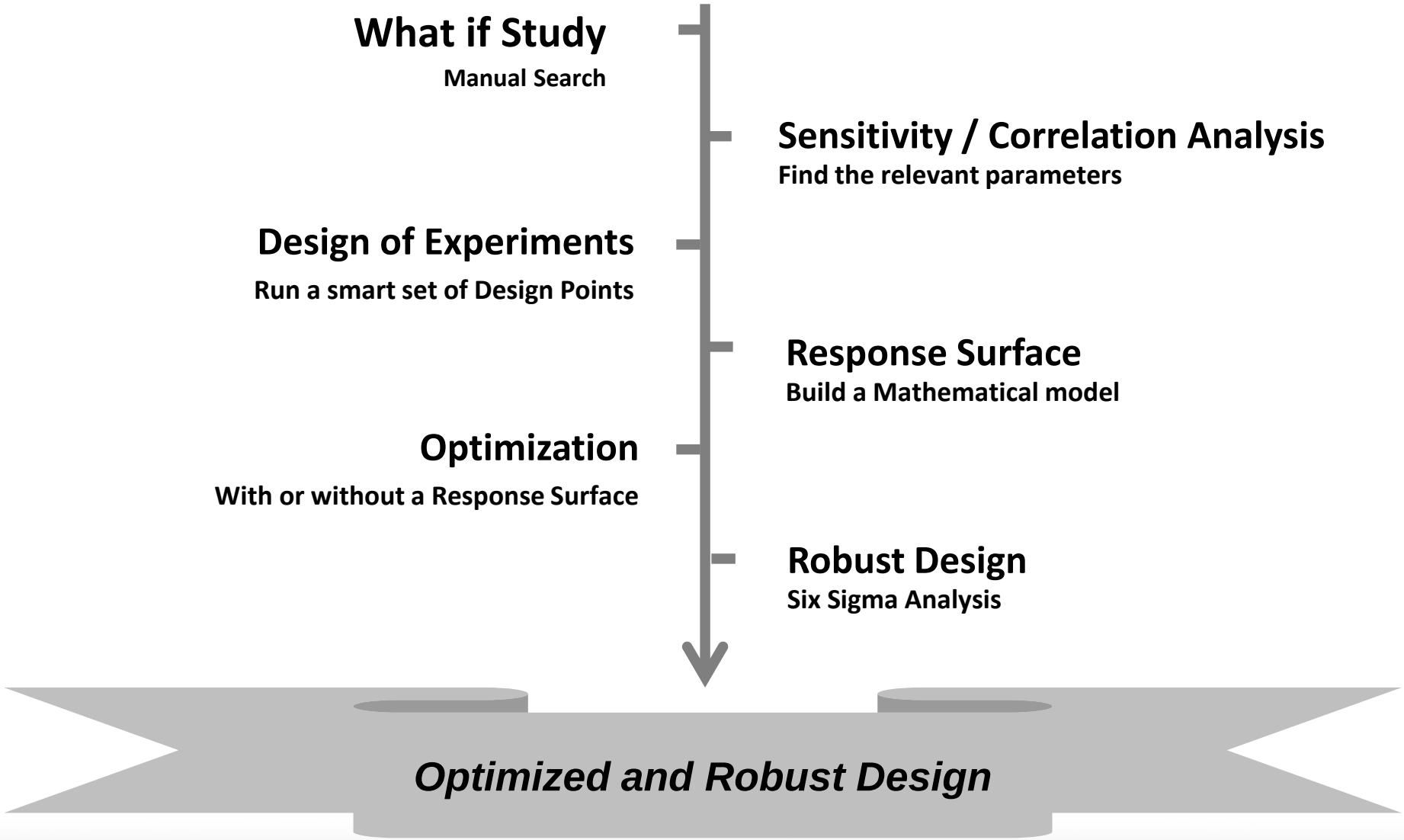






Single Point → ***What If?*** → ***Response Surface***

DesignXplorer Features



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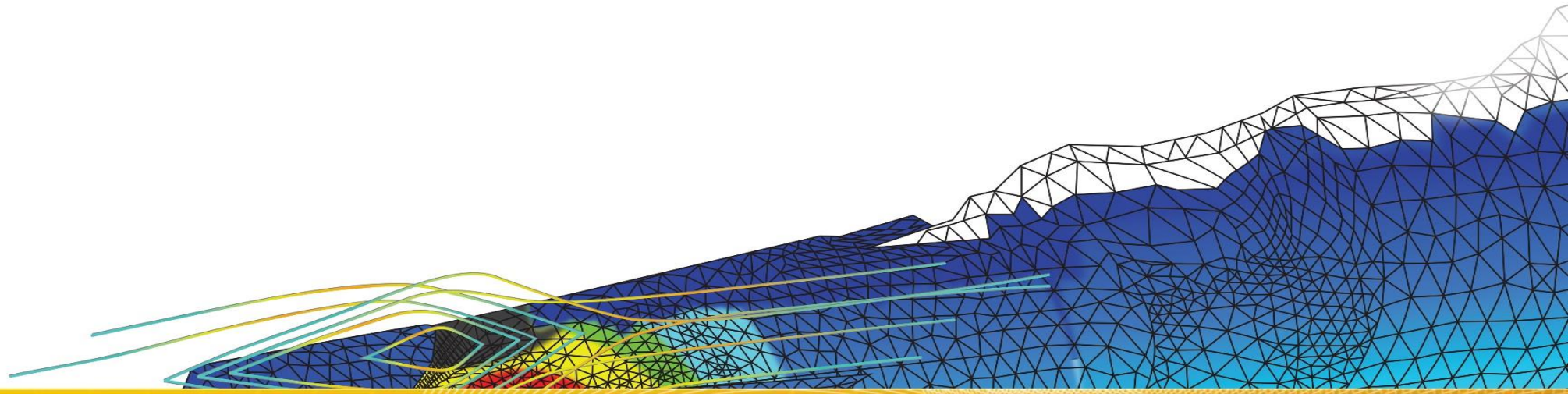
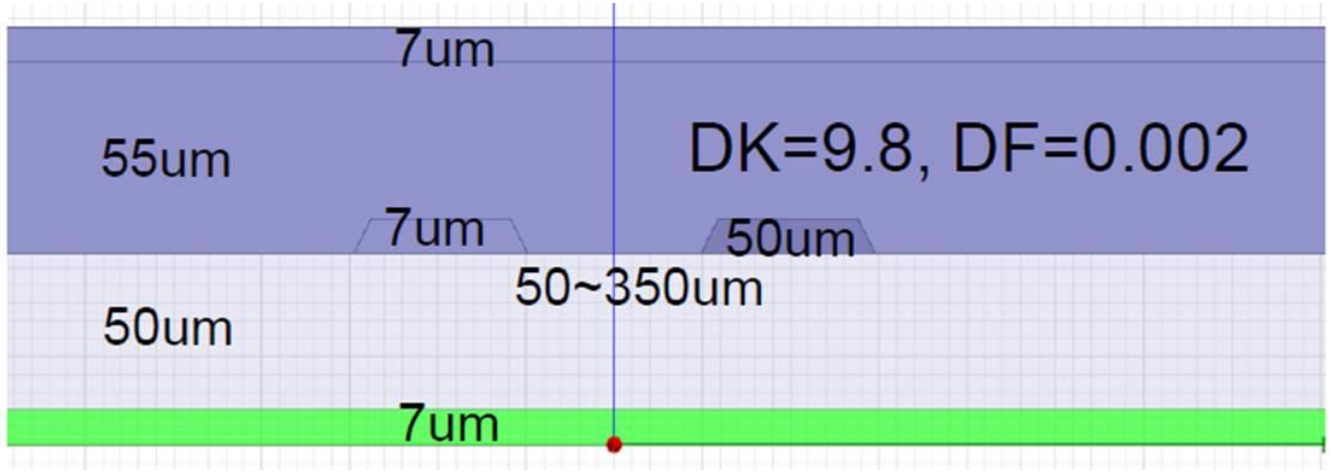
Utilizing Design Space Exploration for Signal Integrity

Pre-layout what-if analysis



Pre-layout what-if analysis

- **Differential stripline study with DesignXplorer**
  –

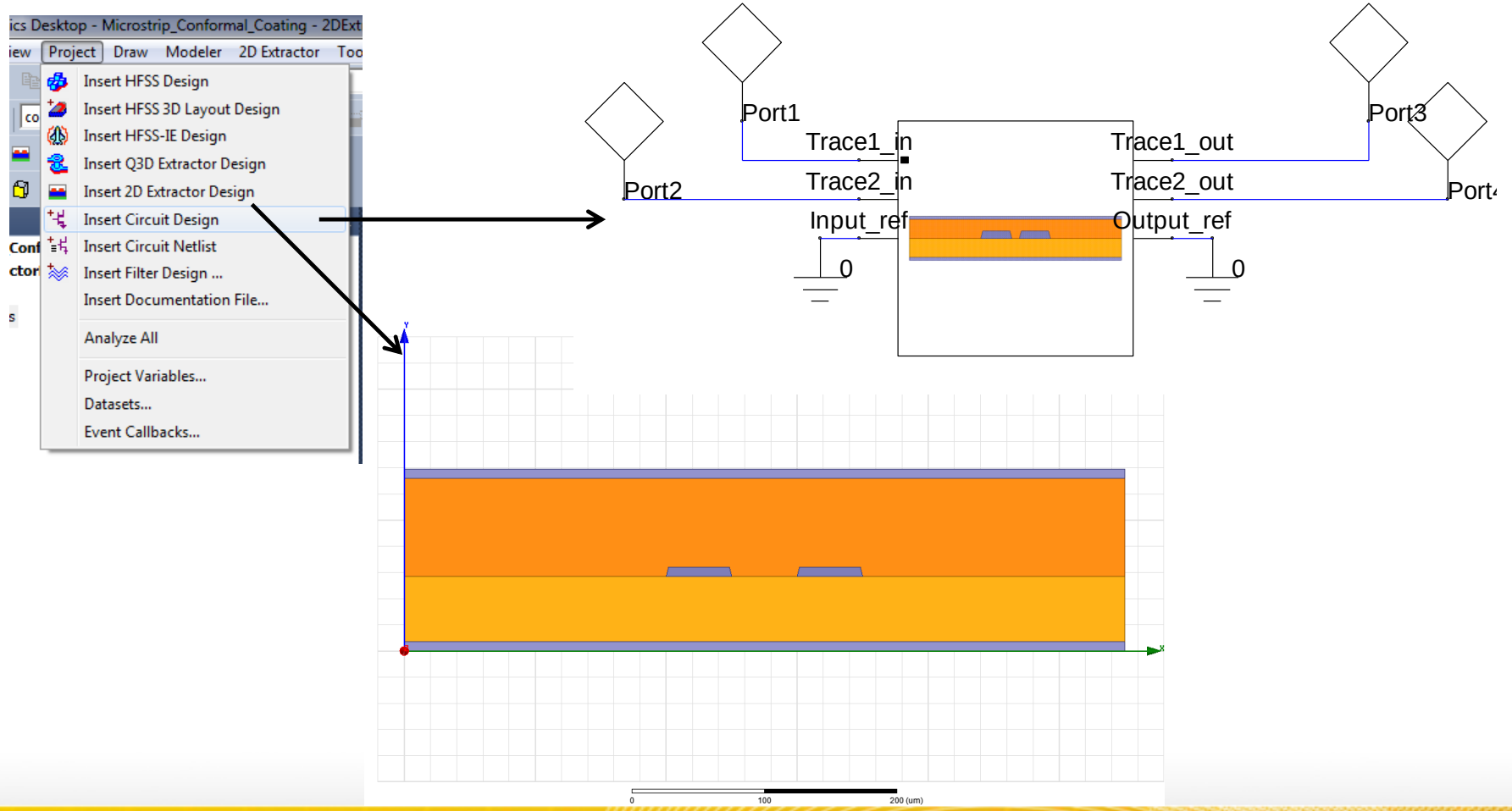


- **Optimization goals**
  - Characteristic Impedance: Z0 (differential) ~ 90 ohm
  - Minimize Insertion loss: >-3dB
  - Maximize Return Loss: <-10dB

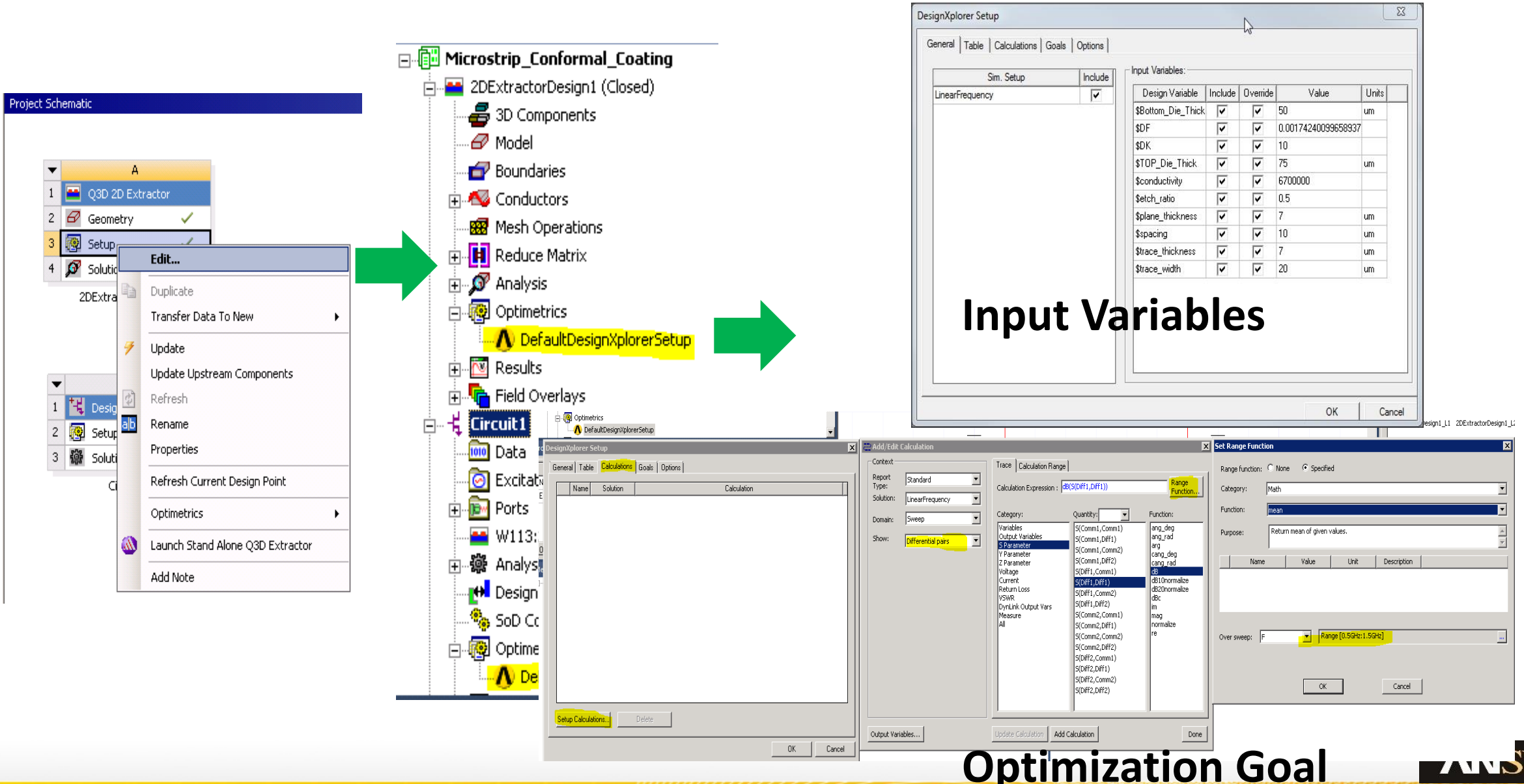
- **Optimization variables**
  - DK=8~10
  - DF=0.0013~0.0024
  - Width=50~80um
  - Seperation=1W~3W
  - Dielectric Thickness: 50~75um
  - Metal Thickness: 7~19um
  - Metal Conductivity: 0.67E7~1.5E7 Siemens/m

Differential stripline model buildup

- **Create a ANSYS Electronics Desktop project with Circuit Design in dynamic linked 2D Extractor**
  - 2D Extractor design: optimize impedance
  - Circuit Design: optimize insertion loss and return loss

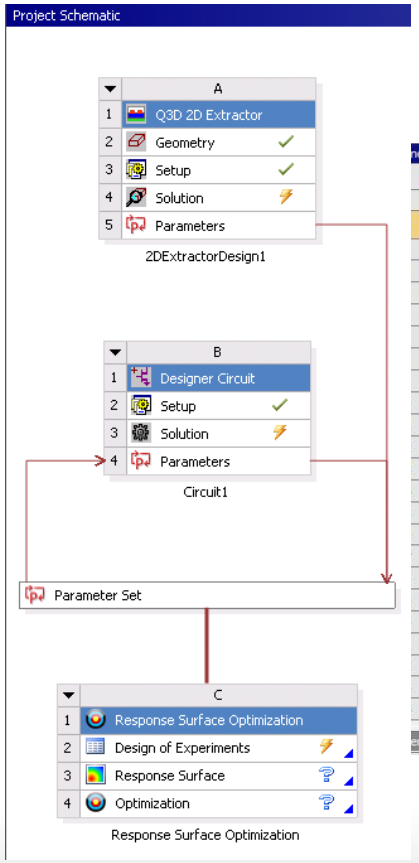


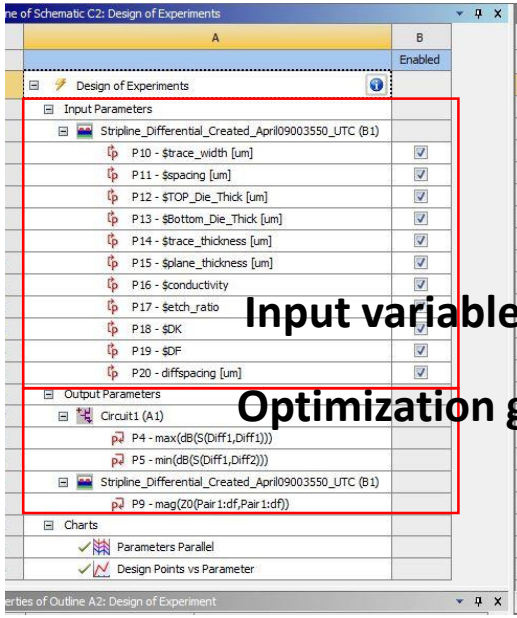
DesignXplorer Response Surface Optimization setup

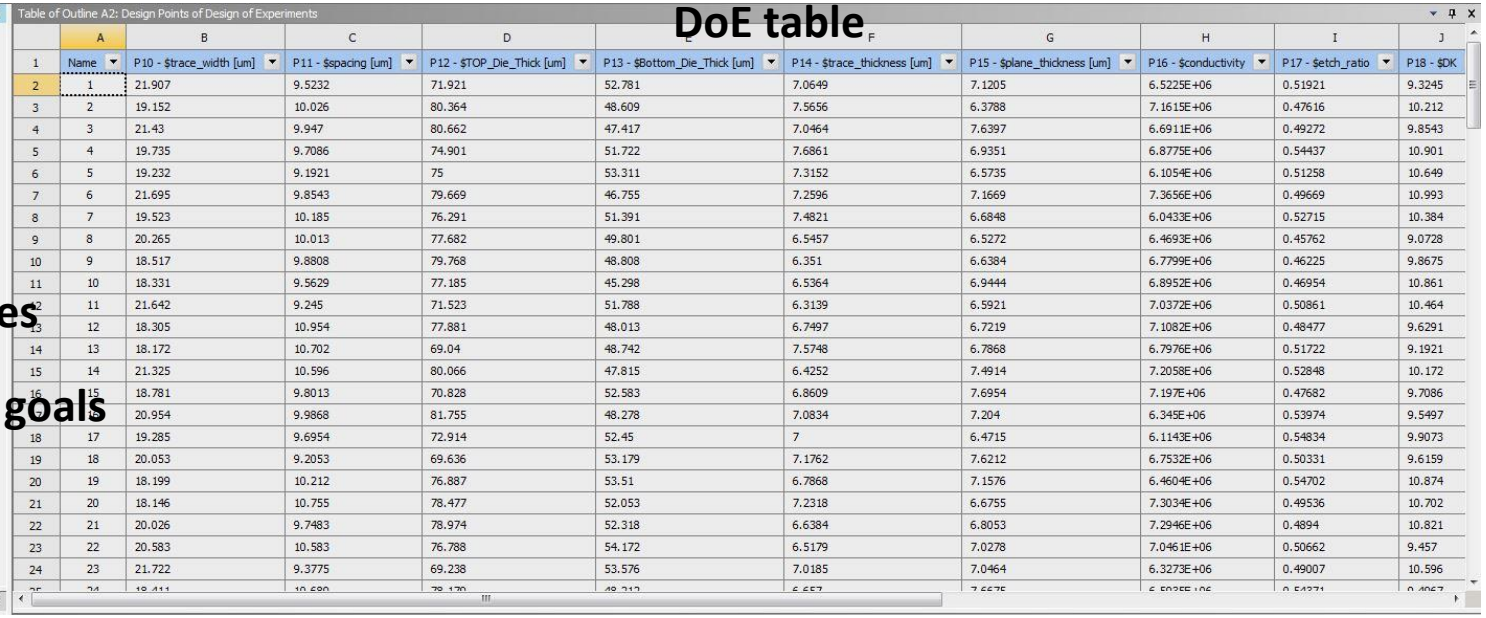


Design of Experiments variable table generation

- **Create Design of Experiments variable table**
  - Specify design variable range setup
  - Preview the Design of Experiments variable table

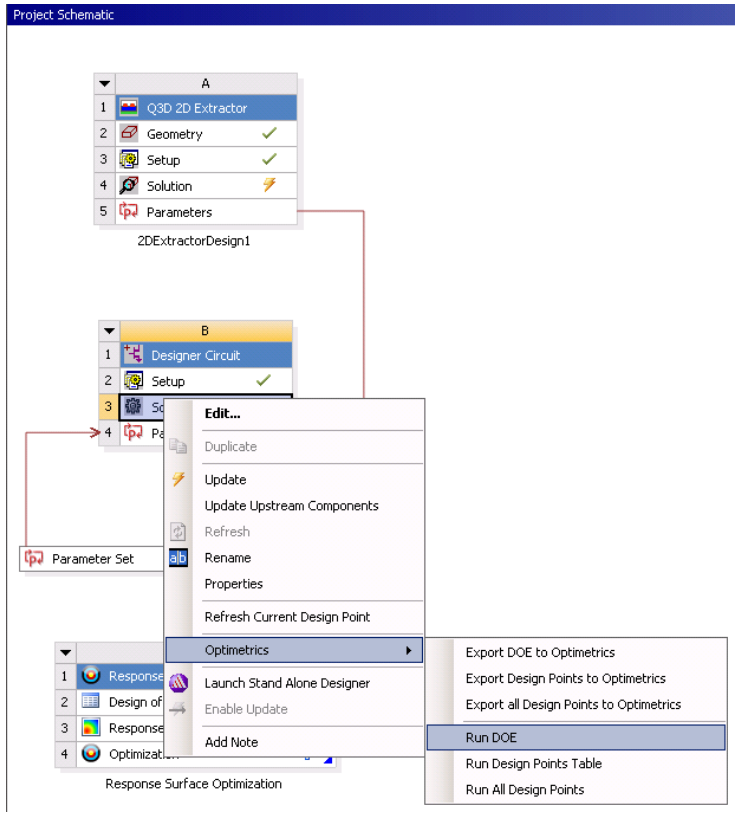






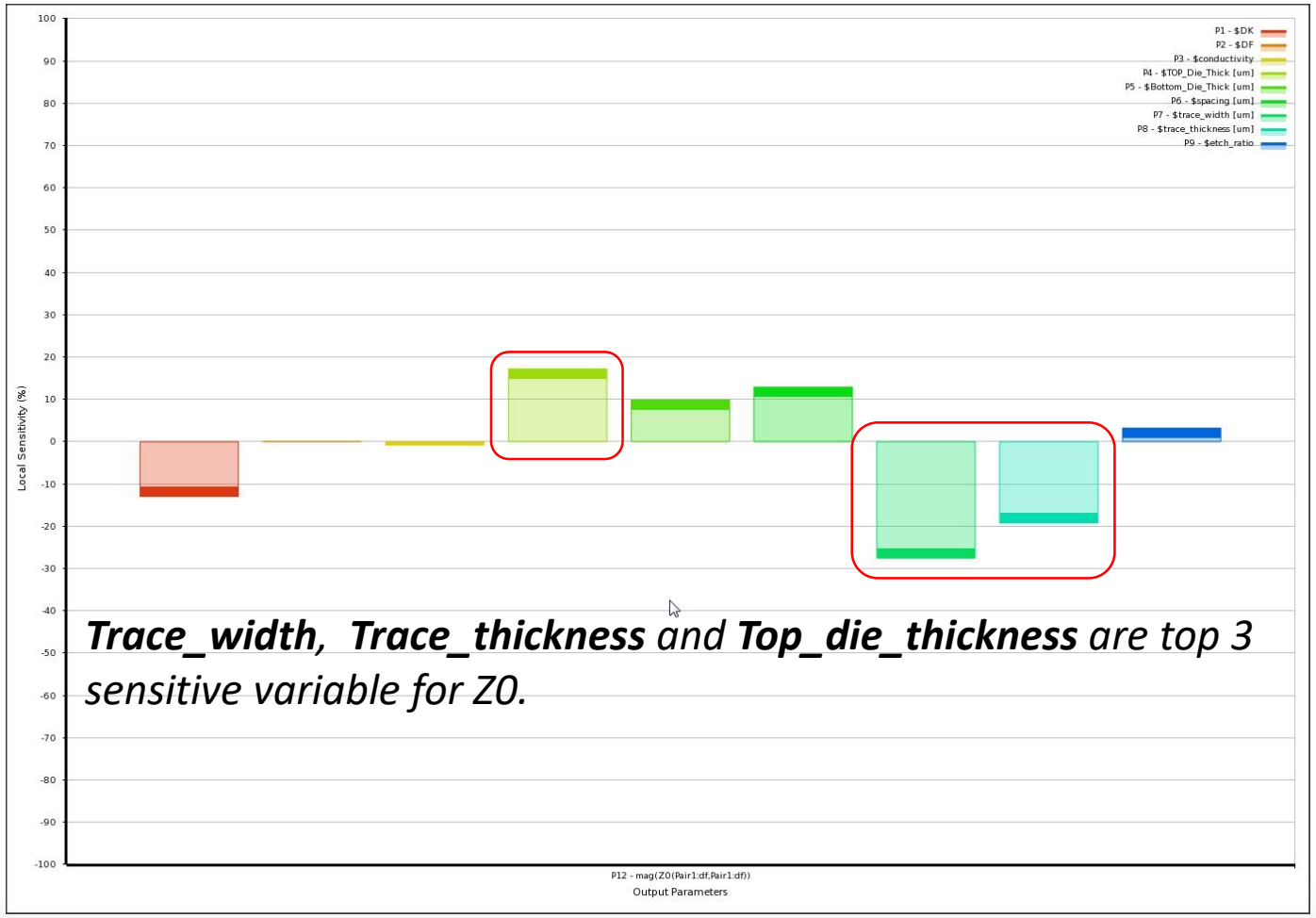
Solve DoE table

- Once the Design of Experiments table is generated, run variable sweeping.
- DSO(Distribution Simulation Option) will distribute variables to multiple nodes to solve simultaneously.



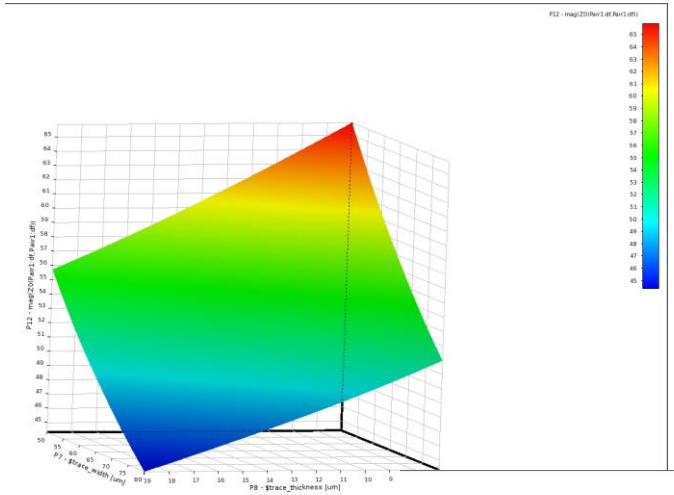
Sensitivity and Response Surface Plots

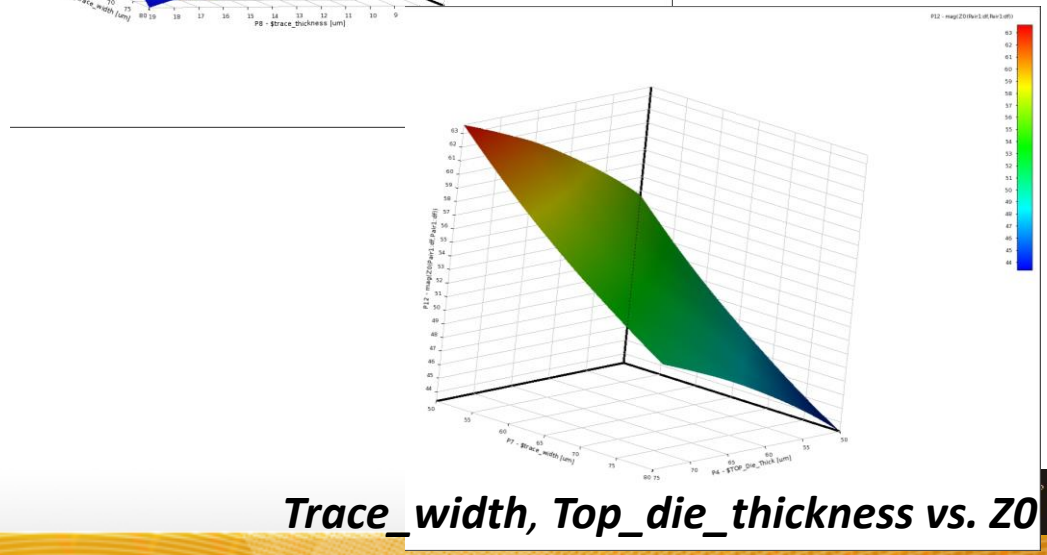
- **Creating Sensitivity and Response Surface for the Design of Experiments results**
  - Sensitivity will display the 2D sensitivity histogram of each input variables vers. output(Z_0).
  - Response displays 3D interaction between variables vers. output (Z_0).



Trace_width, Trace_thickness *and* ***Top_die_thickness*** *are top 3 sensitive variable for Z0.*

Trace_width, Trace_thickness vs. Z0





Trace_width, Top_die_thickness vs. Z0

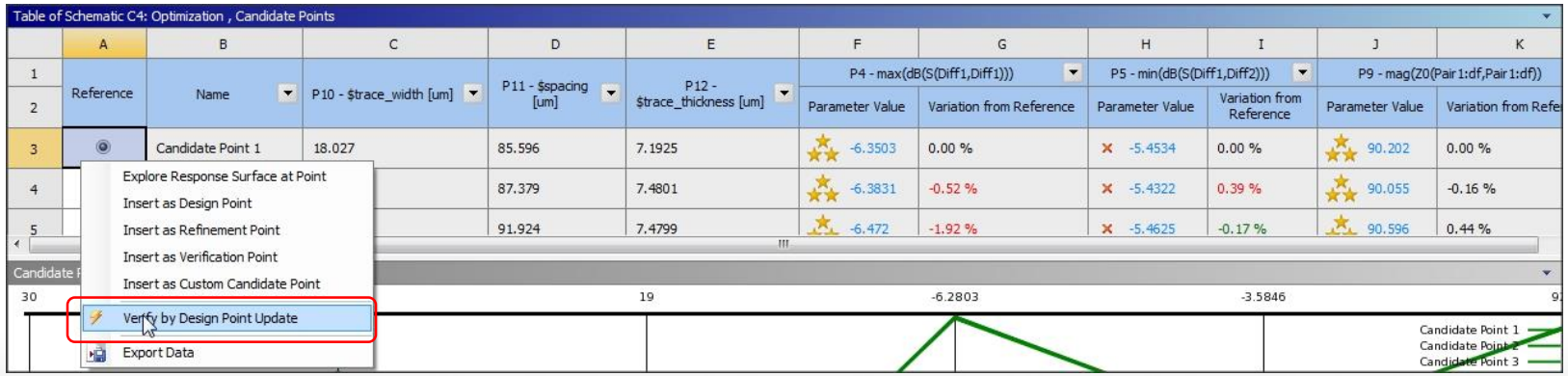
Optimizing over the Response Surface

- **Specify the optimization objectives and constraints**
  - Differential Characteristic impedance of 90 ohm with lower bound 85 ohm and upper bound 95 ohm
  - Maxmimum insertion loss
  - Minimum Return Loss

Table of Schematic C4: Optimization

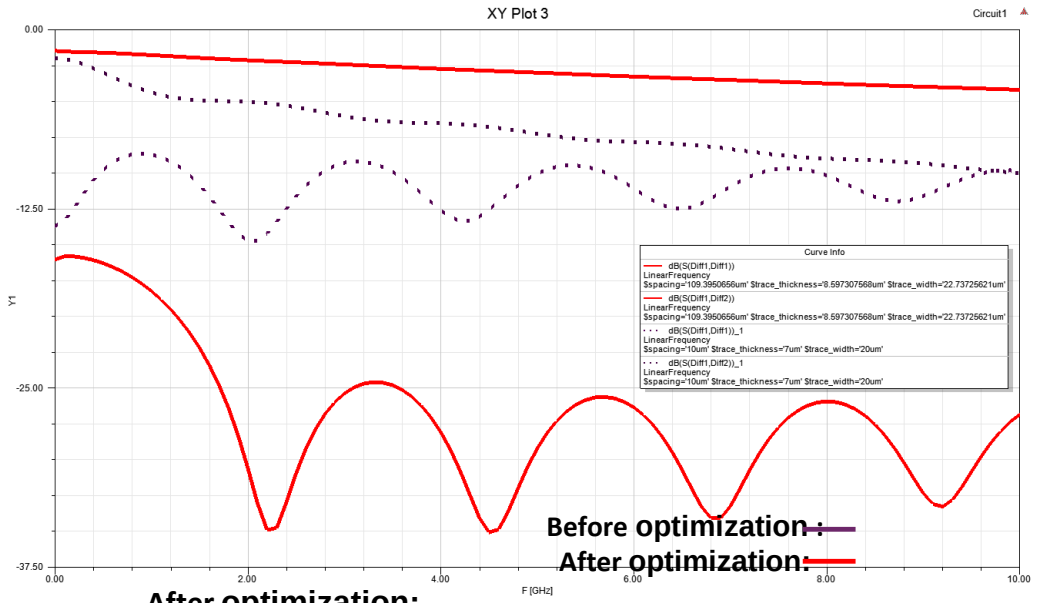
	A	B	C	D	E	F	G
1	Name	Parameter	Objective		Constraint		
2			Type	Target	Type	Lower Bound	Upper Bound
3	Seek P9 = 90; 85 <= P9 <= 95	P9 - mag(Z0(Pair 1:df,Pair 1:df))	Seek Target	90	Lower Bound <= Values <= Upper Bound	85	95
4	Maximize P4	P4 - max(dB(S(Diff1,Diff1)))	Maximize		No Constraint		
5	Minimize P5	P5 - min(dB(S(Diff1,Diff2)))	Minimize		No Constraint		
*		Select a Parameter					

- **The best benefit of the Response Surface approach in DesignXplorer is that the user can change the values of the cost and re-optimize with no further explicit simulations**

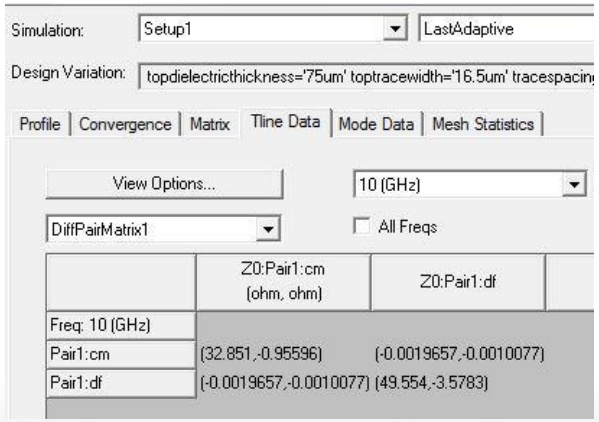


Final Optimized results

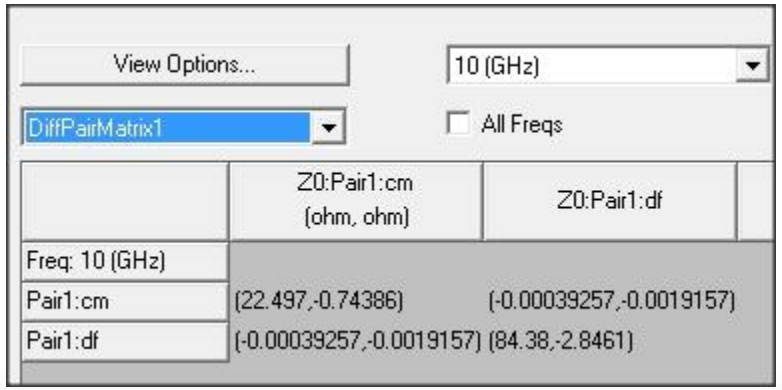
- **After you verify the candidate points, choose the best one for the design**
  - IL&RL:
    - Before optimization: Gray dot line
    - After optimization: Red solid line
  - Differential Character Impedance:
    - Before optimization: 49.5ohm
    - After optimization: 84.3 ohm



Before optimization



After optimization:



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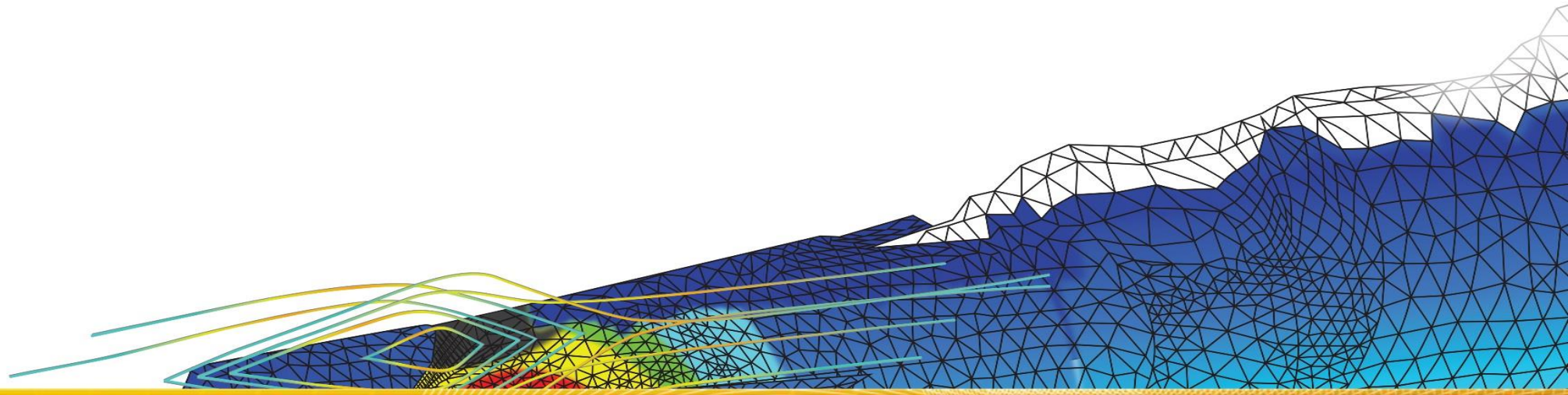
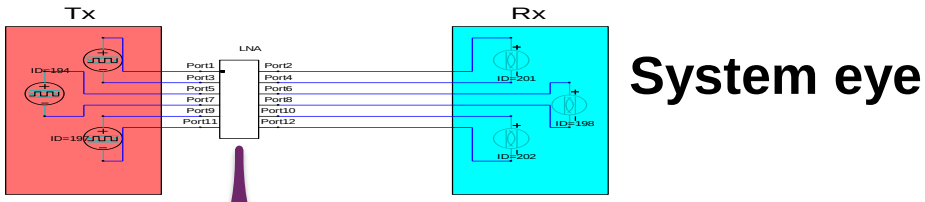
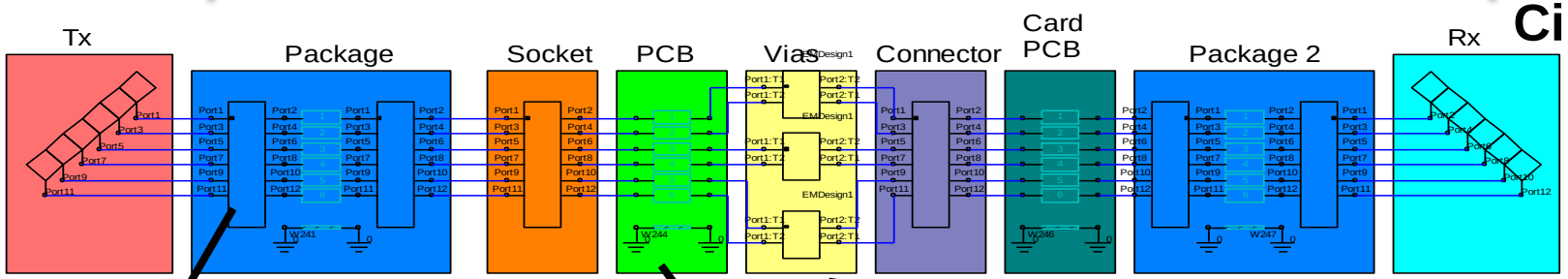
Post-layout Optimization



Hierarchy PCIe Channel Example

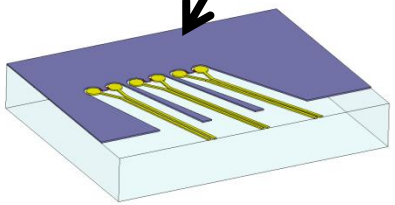


System eye diagram analysis

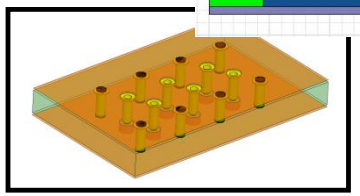


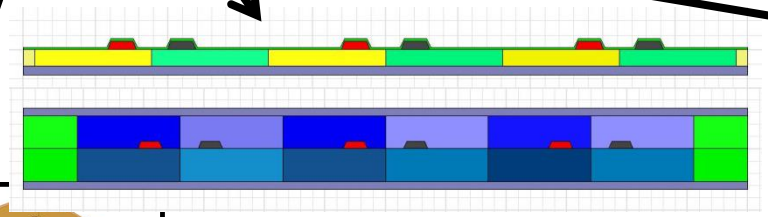
Circuit LNA analysis

Component analysis



HFSS model





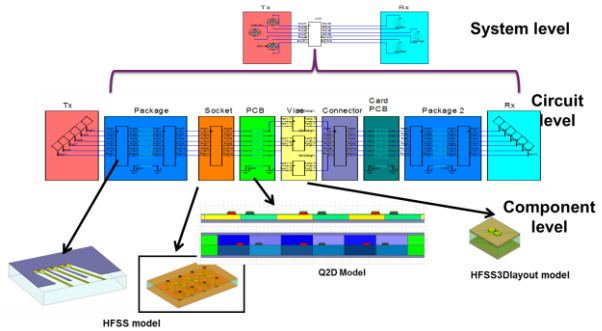
Q2D Model

HFSS3Dlayout model

PCIE Serial Channel Design Problem Scale

30 different factors are unreasonable considering an entire PCIe Channel, for example:

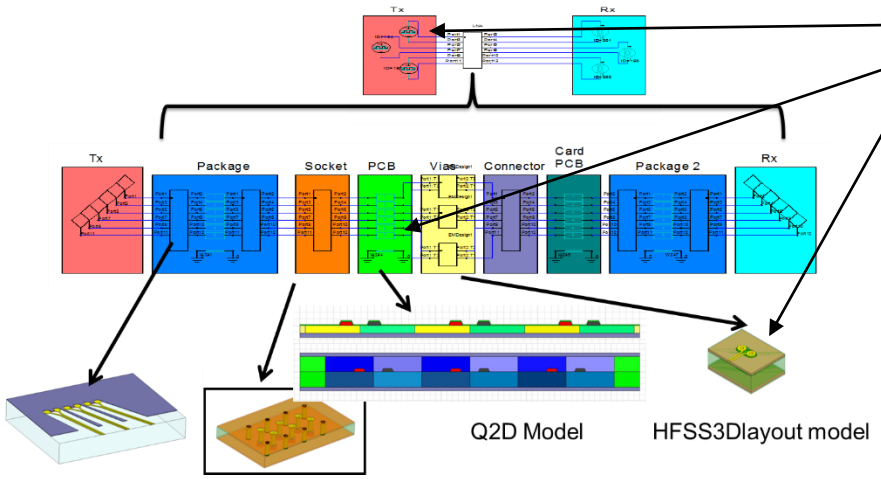
- Package
  - Thickness, Pad breakout, trace length, ball pitch, dielectric material (5)
- Socket
  - Thickness, material properties, SG via ratio (3)
- Board
  - MS and SL trace & space, etch factors, Cu roughness, dielectric materials, via config (8)
- Connector
  - Various vendor models, often only one or two options. (1)
- 2nd Board
  - MS, SL, etch factors, Cu roughness, dielectric materials, via config (8)
- 2nd Package
  - Thickness, Pad breakout, trace length, ball pitch, dielectric material (5)



If each factor has 4 variable value, the total combination scenario will be 120

Different level variables combination affect different level character

- **Sweeping variables**
  - $FFE/DFE level on **System** level (Discrete distribution)
  - $PCB_trace_length on **Circuit** level (Continues distribution)
  - $anti_pad on **Component** level (Continues distribution)



Properties: DOE_eye_Hierarchy

Project Variables | Intrinsic Variables | Constants

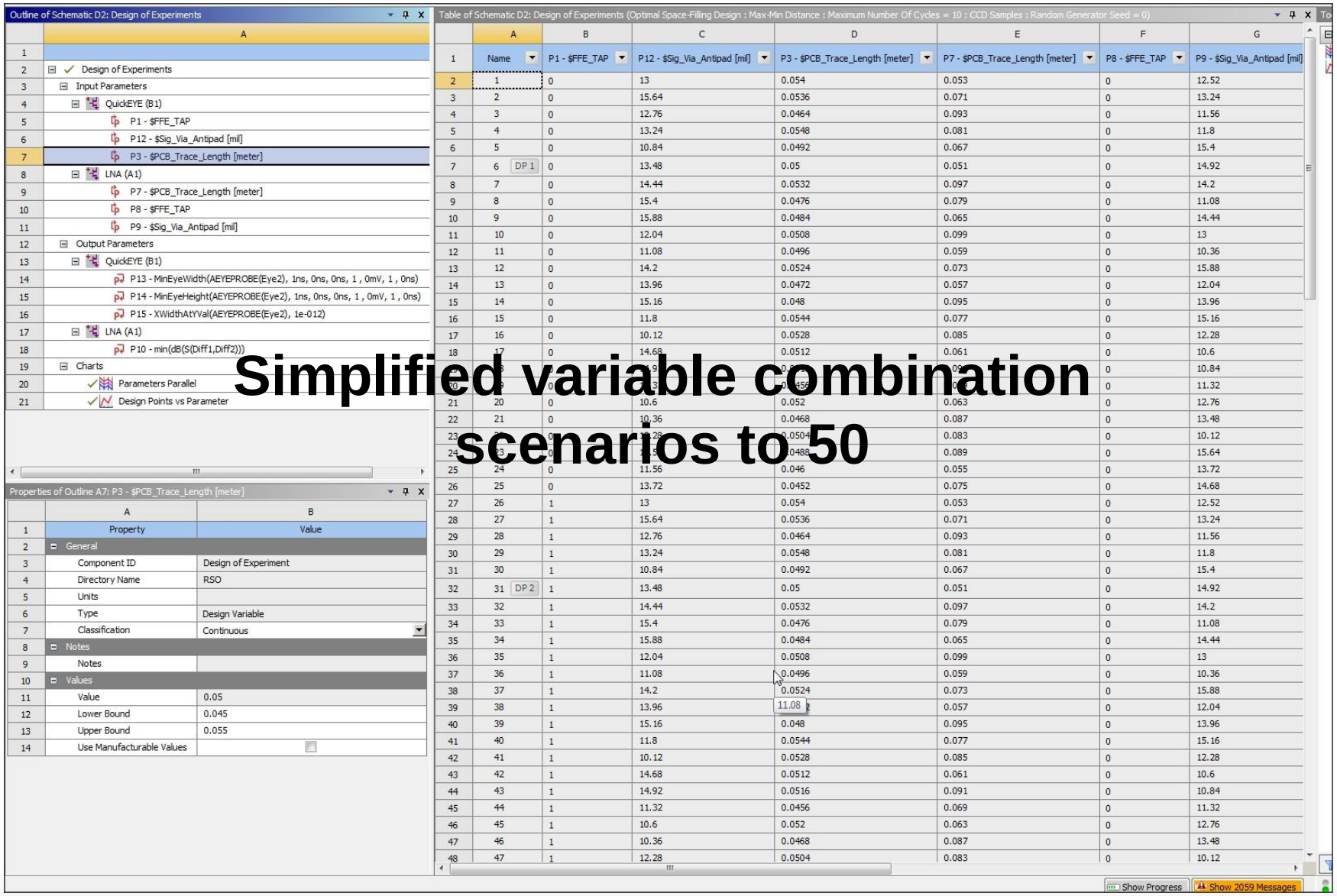
Value | Optimization | Tuning | Sensitivity | Statistics

Name	Value	Unit	Evaluated Value	Description	Read-only	Hidden	Sweep
$Package_trace_length	0.01	meter	0.01meter				
$Socket_Array_Index	0		0				
$PCB_Array_Index	0		0				
$Via_Model_Array_Index	0		0				
$Card_trace_length	0.01	meter	0.01meter				
$FFE_TAP	2		2				
$PCB_Trace_Length	0.05	meter	0.05meter				
$antiPad	770	um	770um	Signal via antipad diam...			
$GND_Via_Pad	30	mil	30mil				
$GND_Via_Anitpad	25	mil	25mil				
$GND_Via_Drill	12	mil	12mil				
$Sig_Via_Pad	20	mil	20mil				
$Sig_Via_Antipad	10	mil	10mil				
$Sig_Via_Drill	8	mil	8mil				
$SM_Top	0.9	mil	0.9mil				
$L1_THK	0.7	mil	0.7mil				
$D1_THK	4	mil	4mil				
$L2_THK	0.7	mil	0.7mil				
$D2_THK	4	mil	4mil				
$L3_THK	0.7	mil	0.7mil				
$D3_THK	4	mil	4mil				
$L4_THK	0.7	mil	0.7mil				
$D4_THK	4	mil	4mil				
$L5_THK	0.7	mil	0.7mil				
$D5_THK	4	mil	4mil				
$L6_THK	0.7	mil	0.7mil				
$D6_THK	4	mil	4mil				
$L7_THK	0.7	mil	0.7mil				
$D7_THK	4	mil	4mil				
$L8_THK	0.7	mil	0.7mil				
$SMB_THK	0.9	mil	0.9mil				
$Socket_Array	["$PROJECTDIR\Socket\Socket_1_6_SG...		["$PROJECTDI...				
$PCB_Array	["Diff_SL_76_Ohm_20mil_Spacing", "Diff_S...		["Diff_SL_76_O...				
$Via_Model_Array	["$PROJECTDIR\Via_Models\Via_L14_0_...		["$PROJECTDI...				

- **Optimization goal:**
  - **BER** for statistic analysis
  - **Eye width/height** for statistic/circuit analysis(timing domain)
  - **Insertion loss/Return loss** for circuit analysis(frequency domain)

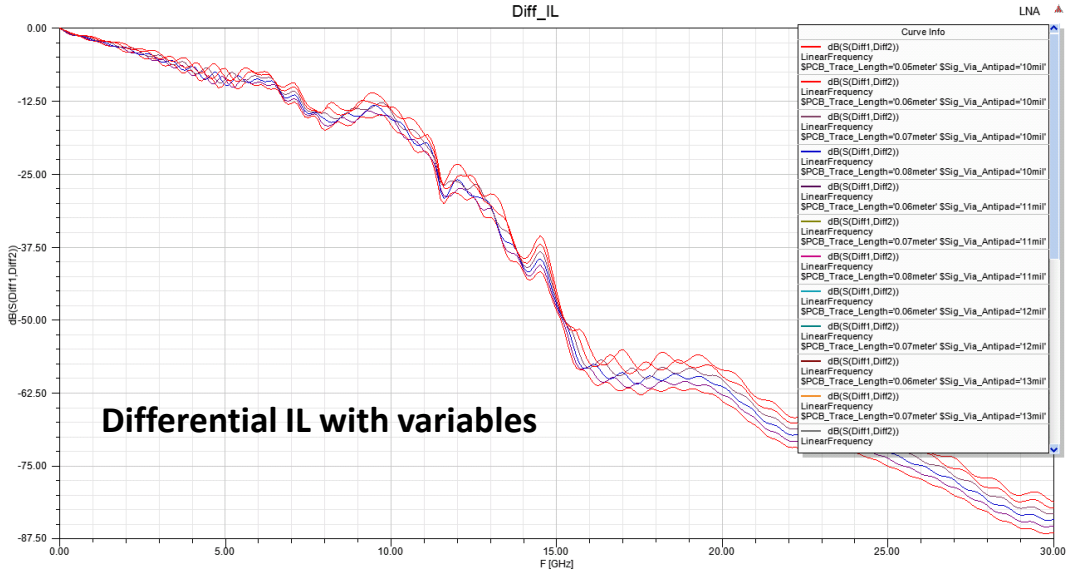
11	P9 - $Sig_Via_Antipad [mil]
12	Output Parameters
13	QuickEYE (B1)
14	P13 - MinEyeWidth(AEYEPROBE(Eye2), 1ns, 0ns, 0ns, 1 , 0mV, 1 , 0ns)
15	P14 - MinEyeHeight(AEYEPROBE(Eye2), 1ns, 0ns, 0ns, 1 , 0mV, 1 , 0ns)
16	P15 - XWidthAtYVal(AEYEPROBE(Eye2), 1e-012)
17	LNA (A1)
18	P10 - min(dB(S(Diff1,Diff2)))

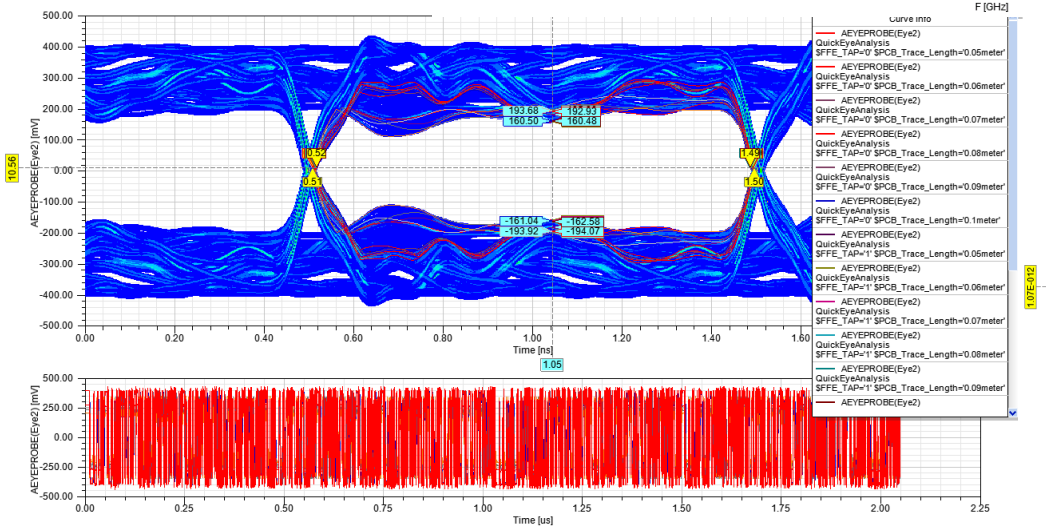
PCIe Channel DoE data table



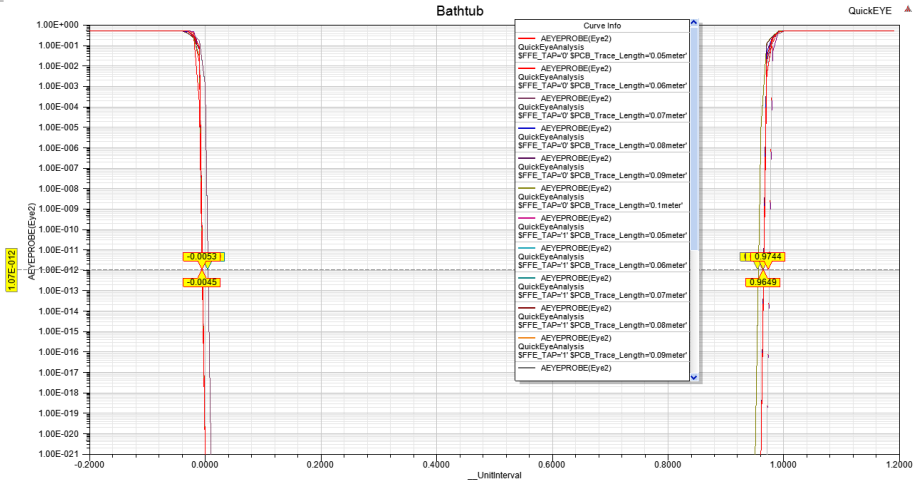
Simplified variable combination scenarios to 50

PCIe Channel Example – View the swept output



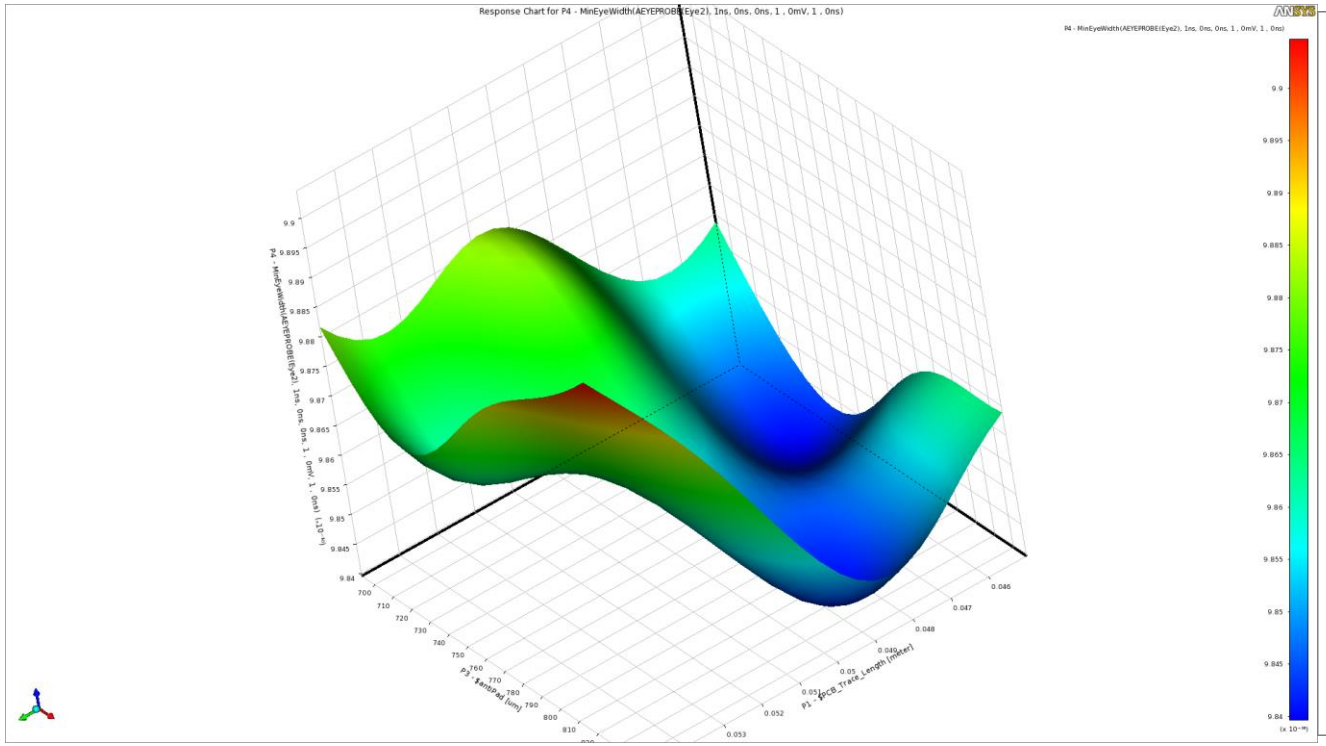


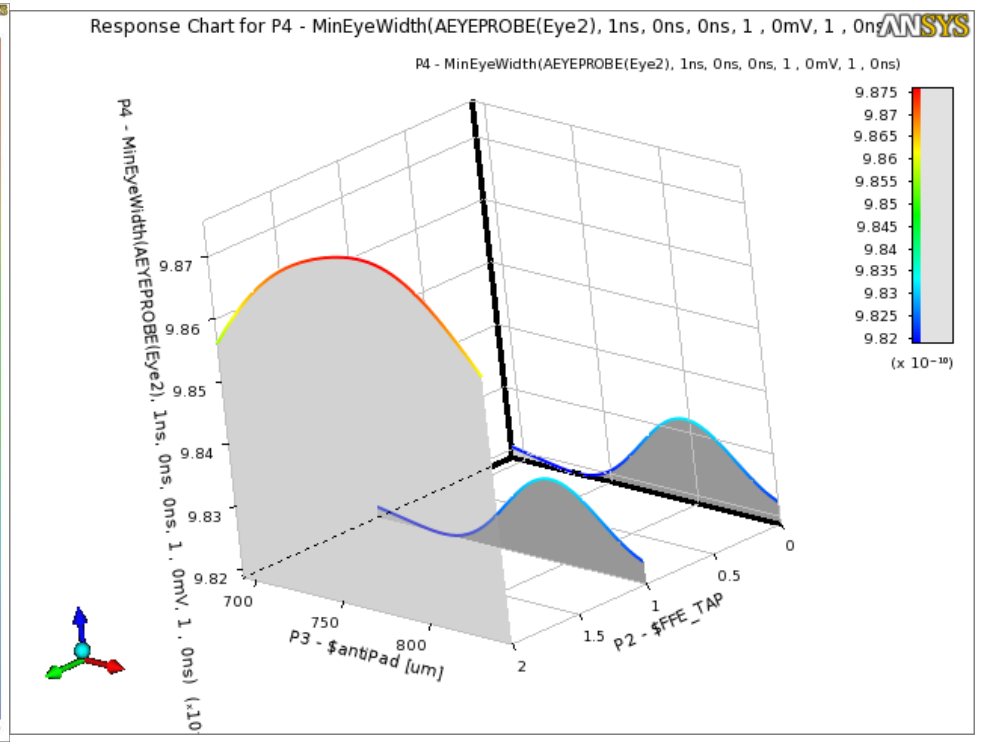
Eye diagram with variables



Bathtub with variables

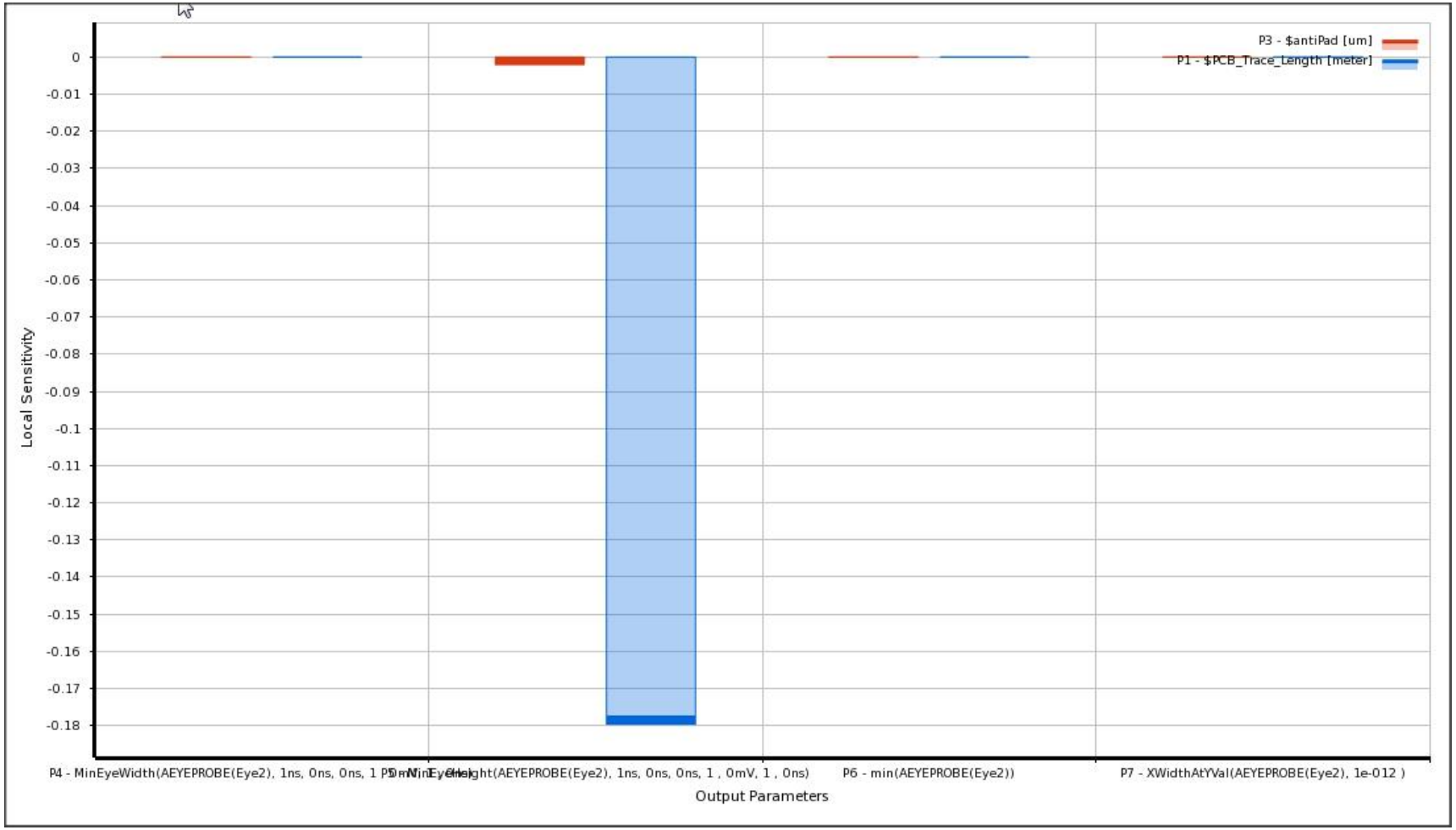
Response Surfaces





- Visualize response surfaces in 3D or 2D plots (continuous, discreet, mixed) variables
- The Measure of fit provides a metric for evaluating the accuracy of the response surface model.
- 3D: ***Eye Width*** vs. ***PCB tracelength& antipad size /Eye Width vs. FFE& Antipad size***

Sensitivity Plots

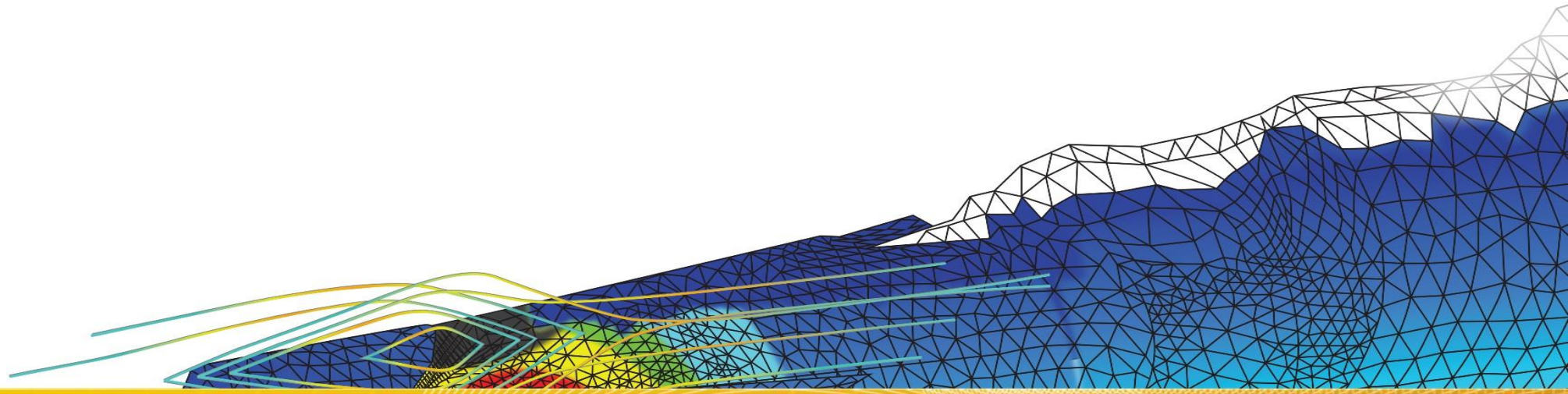


Sensitivity histogram shows that ***$Trace_length*** is the most sensitive parameter for ***Eye_width***

ANSYS®

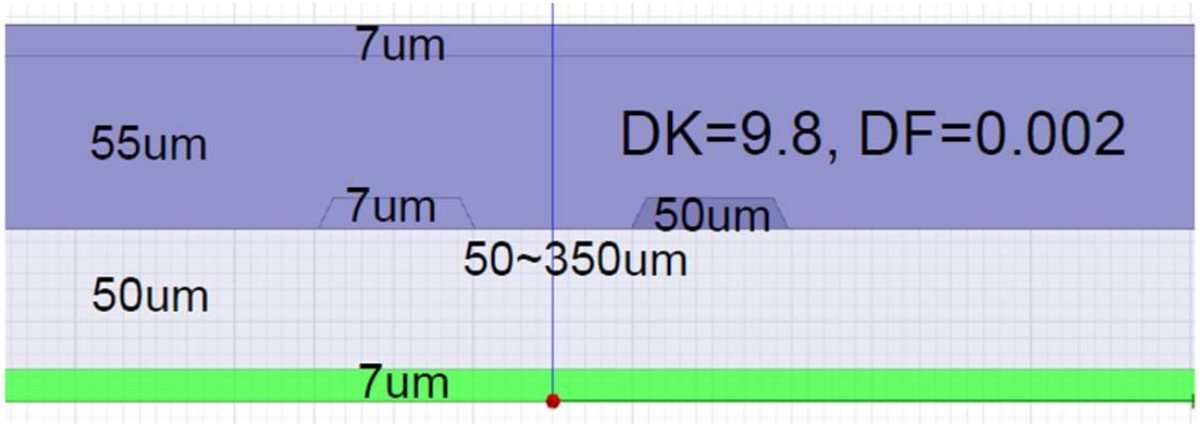
Utilizing Design Space Exploration for Signal Integrity

Manufacture tolerance study (6σ-six sigma)



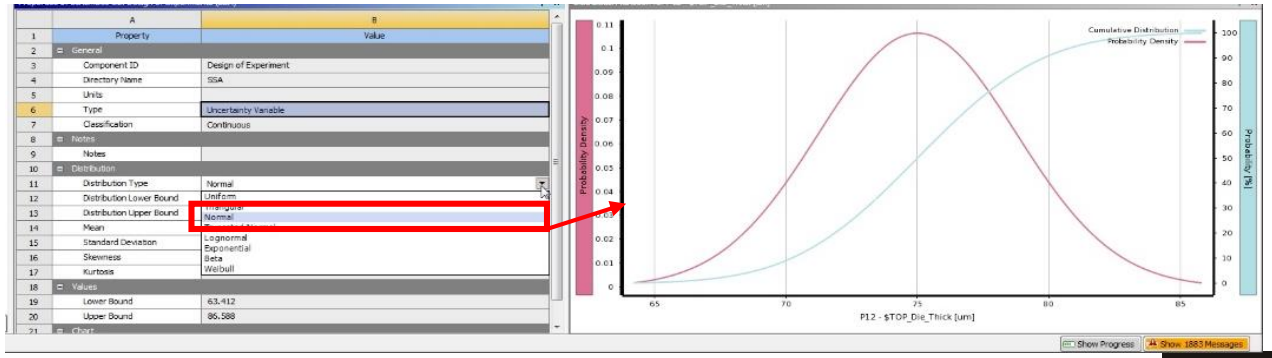
DesignXplorer for PCB manufacture tolerance study example

- **Differential stripline study with DesignXplorer**
  - 6σ analysis will be done based on user defined variable range and distribution

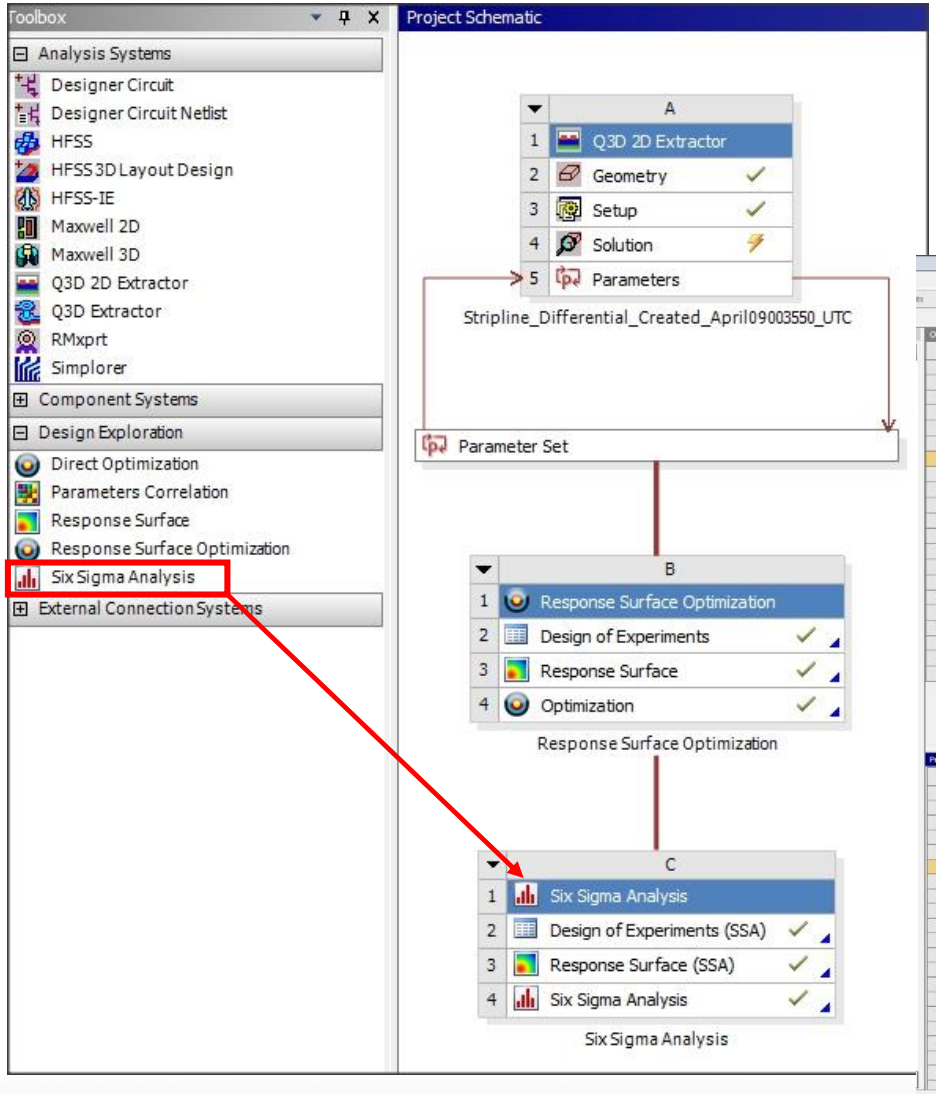


- **Manufacture variables**
  - DK=8~10
  - DF=0.0013~0.0024
  - Width=50~80um
  - Seperation=1W~3W
  - Dielectric Thickness: 50~75um
  - Metal Thickness: 7~19um
  - Metal Conductivity: 0.67E7~1.5E7 Siemens/m

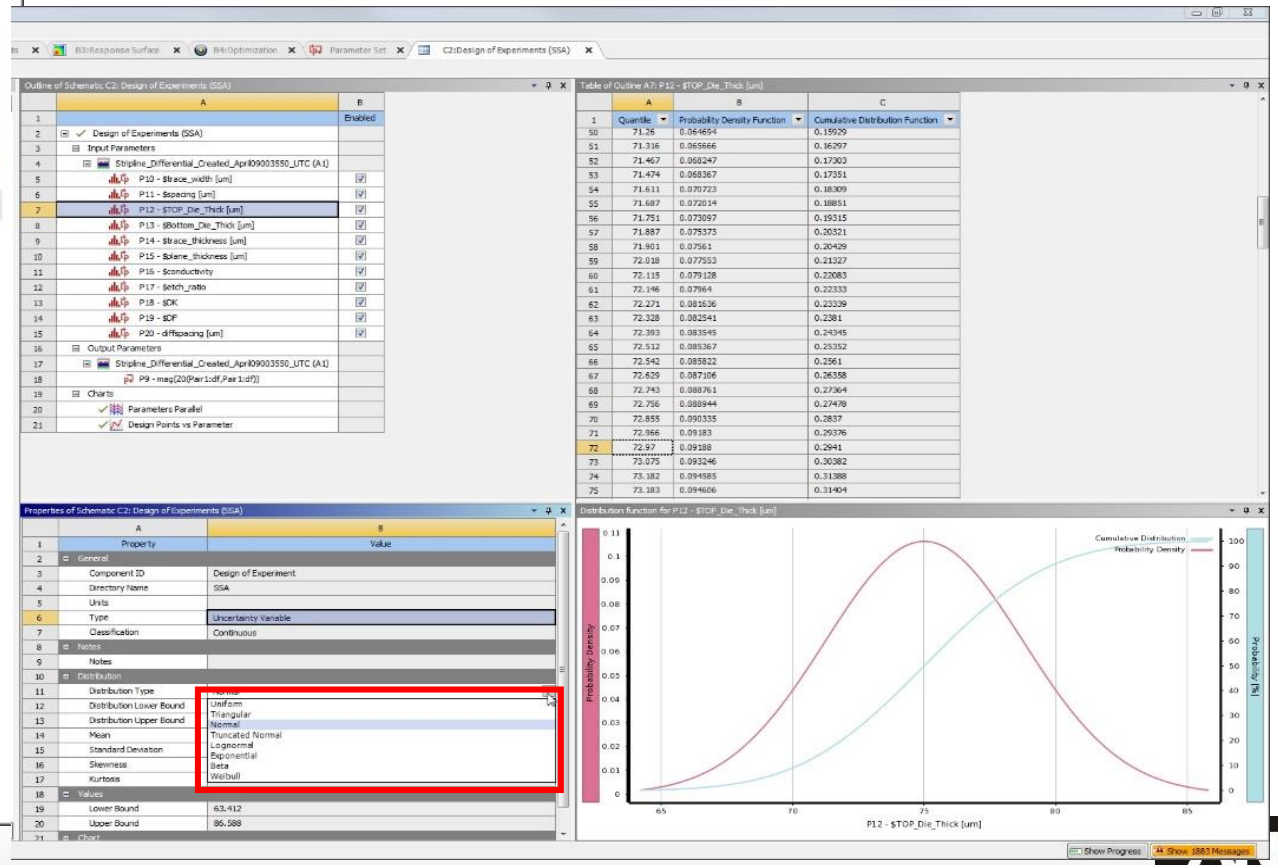
All variables are Normal (Gaussian) distribution



6σ Analysis

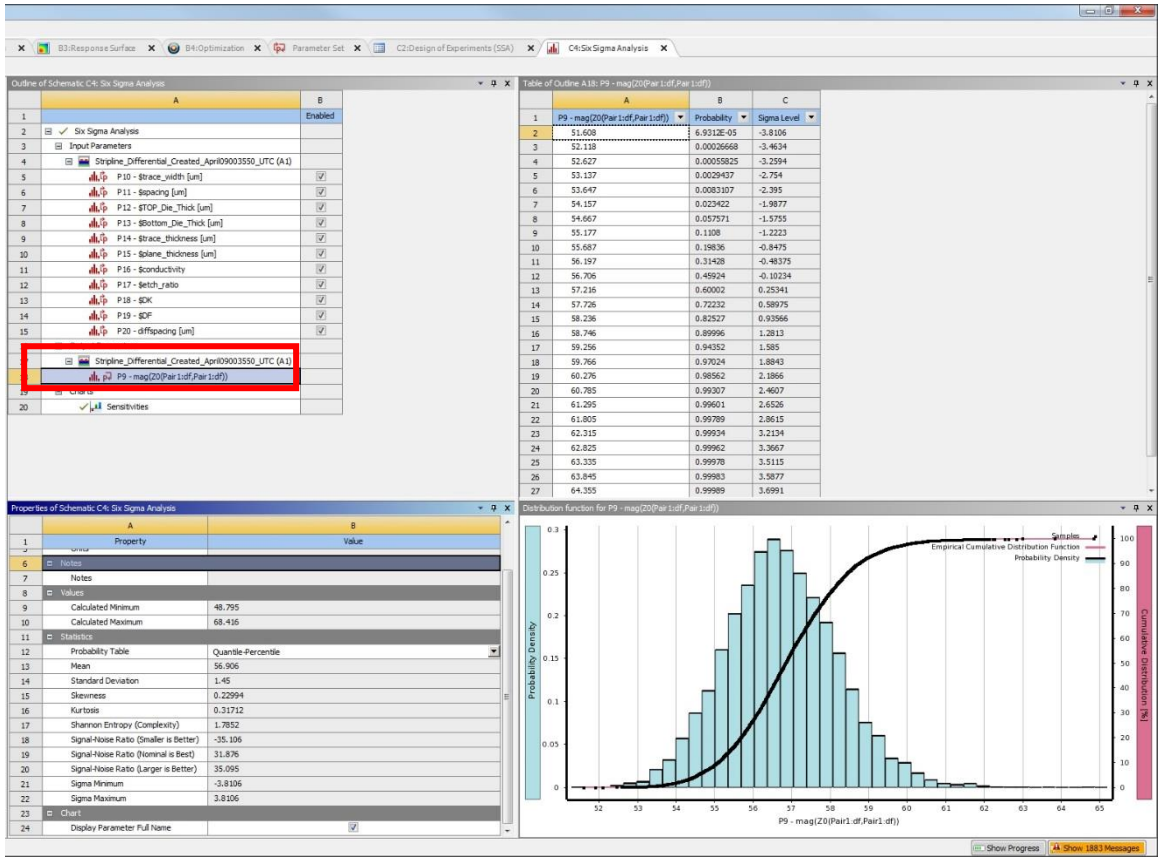


6σ analysis is continuously studying, specifying each variable bounder and distribution.



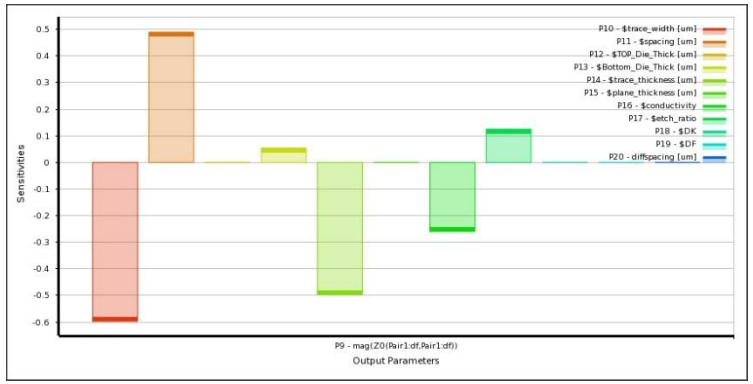
6σ Analysis results

- **6σ analysis will give statically distribution function and relative sensitivity curve.**



The mean value was 48.79 ohm, peak value was 51.31ohm(min) and 68.47ohm(max)

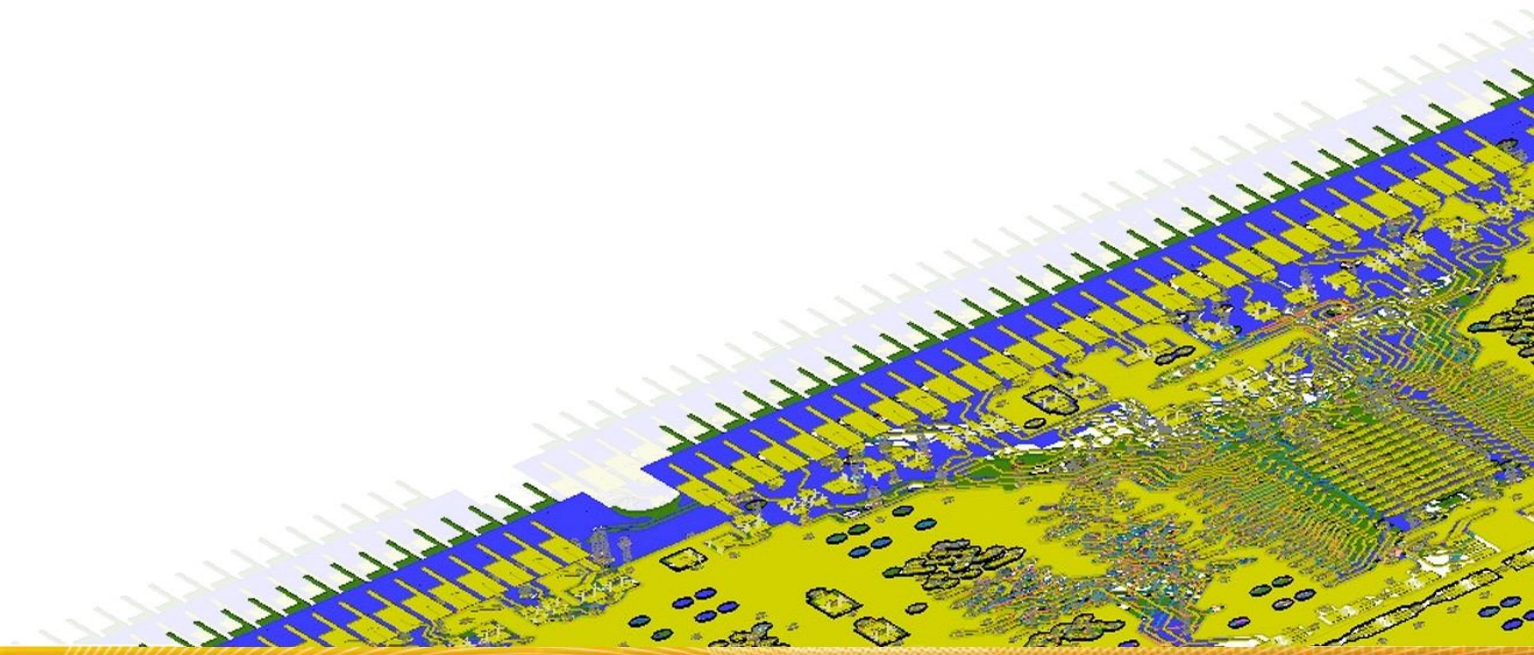
Probability density distribution



Relative Sensitivity results

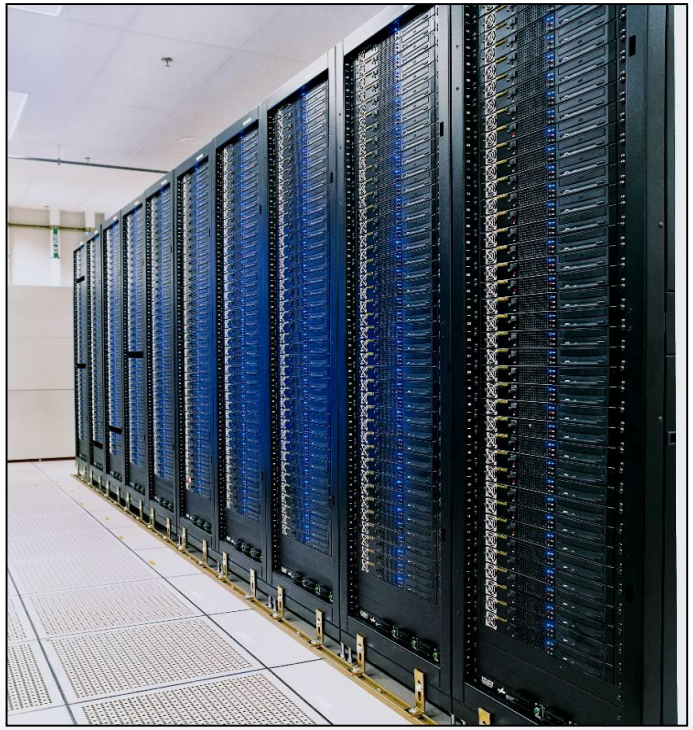
ANSYS®

Full Hardware Utilization for Design Space Exploration



HPC: High Performance Computing

- HPC enables increased productivity and higher fidelity simulation - including more geometric detail and larger systems.
- HPC helps you make your product development process, more productive and efficient.
- Faster turnaround and larger models all mean better designs in less time.



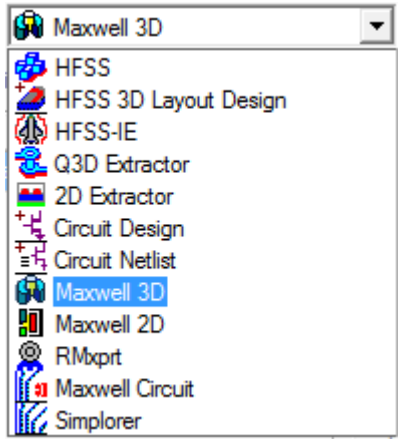
Faster

Bigger

Higher Fidelity

How to Enable HPC Pool License ?

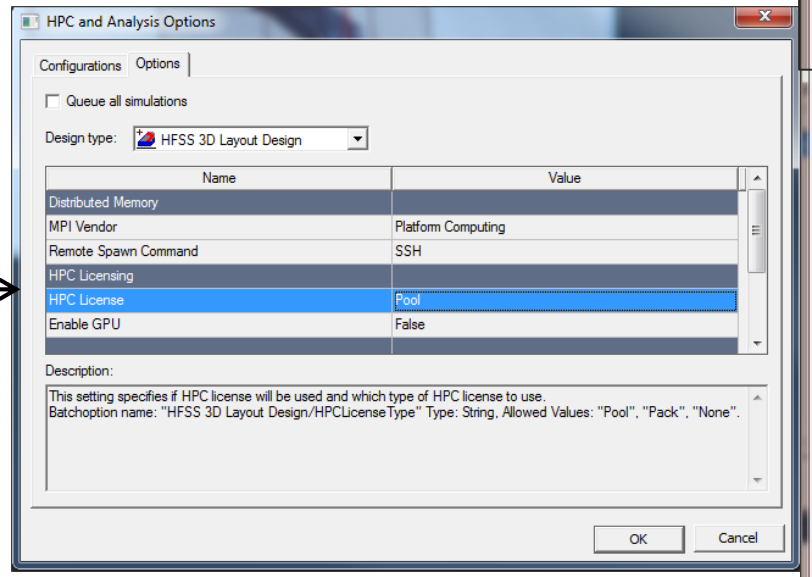
- **Tools > Options > HPC and Analysis Options**
- **Design Type:**

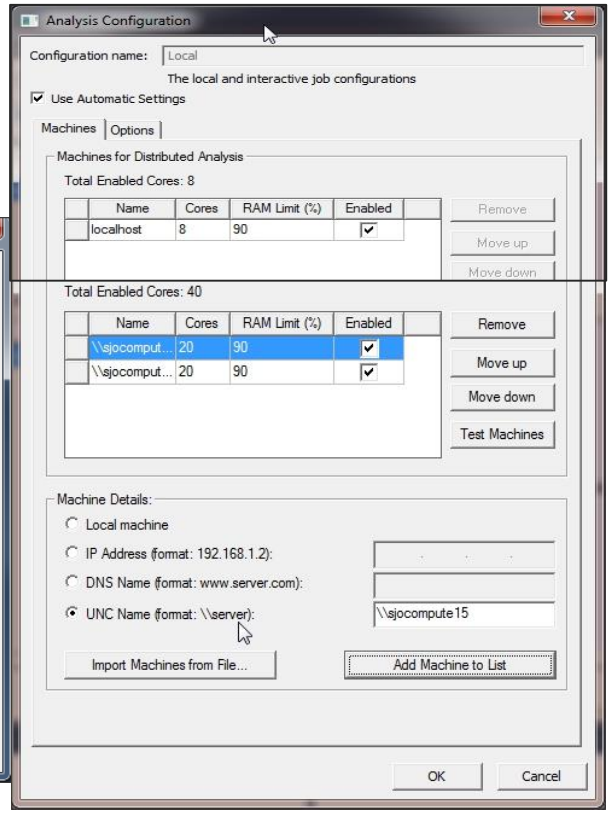


- **Specify more than 1 cores**
- **Options Tab**
  - HPC License - Pool

Enable HPC Pool

HPC = Faster





Apple had 1536 tasks EM HPC workgroup license

DSO: Distributed Solve Option

Distributed Solve Option

Distributed Solve Option

- Enables multiple ***parametric variations*** to be solved simultaneously on local and/or networked cores
- Each variable will utilize same HPC setting, which offers a near-linear speed-up with the number simultaneous variations (DSO tasks)
- Key for accelerating robust design (design of experiments, six sigma, etc.)

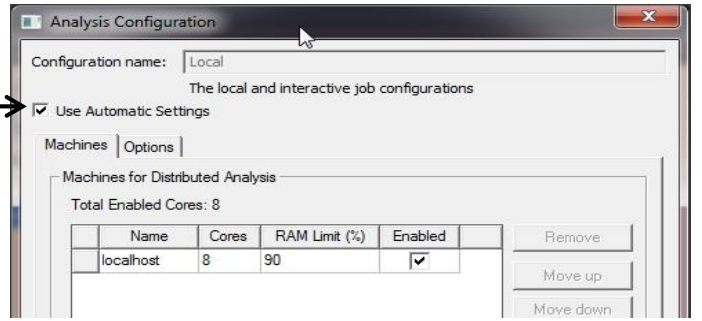
Design Space

Faster

How to Enable DSO License ?

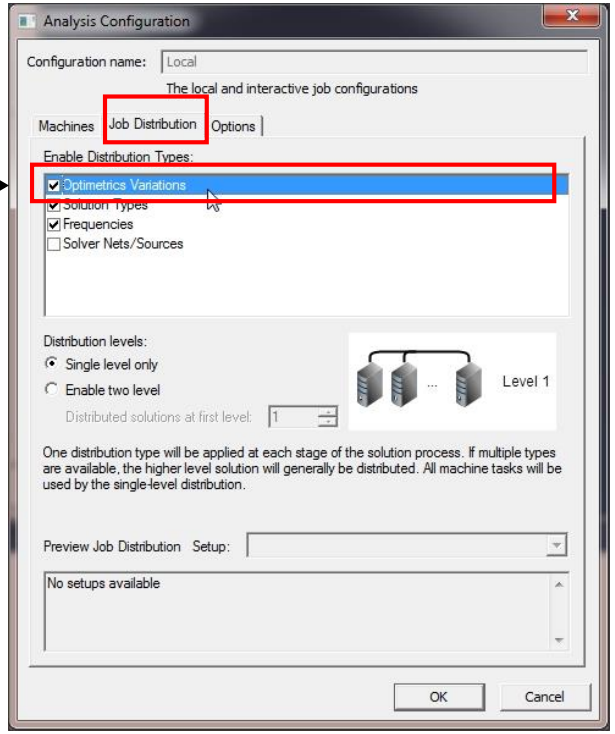
- **Tools > Options > HPC and Analysis Options**
  - HFSS, HFSS-IE and HFSS 3Dlayout:
    - DSO is enable if check ***Use automatic settings***

HFSS, HFSS-IE, HFSS3Dlayout Enable DSO



  - Q2D/Q3D, Maxwell, Circuit and Simplorer:
    - In ***Job Distribution*** tab, checking **Optimetrics Variations** to enable DSO

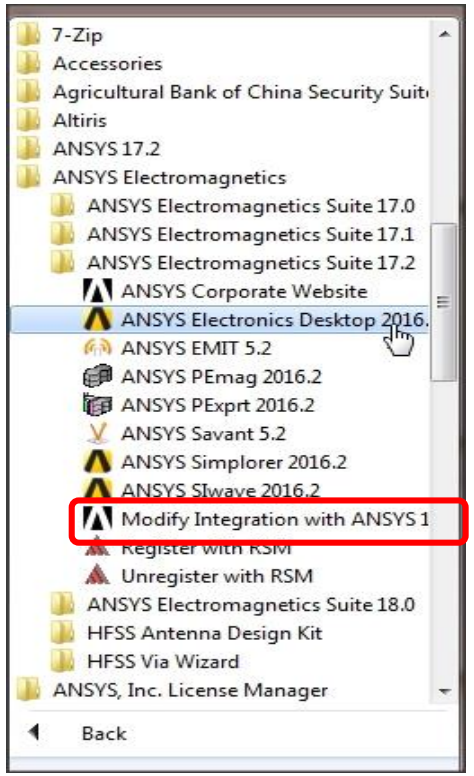
Q2D/Q3D, Maxwell, Circuit, Simplorer Enable DSO



Apple had 211 tasks DSO license

Software and License requirements

- **Software Requirements**
  - ANSYS Electronic Desktop 2016.2 (ANSYS EM Suite 17.2)
  - ANSYS Workbench 17.2 with Pre/Post
  - Integrated ANSYS Electronic Desktop with Workbench
- **License**
  - ANSYS HFSS with SI options
  - Optimetrics
  - HPC
  - DSO
  - ANSYS DesignXplorer



Conclusion

- ANSYS provides unified platform for Signal Integrity Design Space Exploration, which covers pre-layout, post-layout simulation and manufacture tolerance study.
- DesignXplorer gives easy way to automatically set up SI for Design Space exploration and Optimization
- HPC and DSO will utilize all of the available hardware to accelerate simulation.