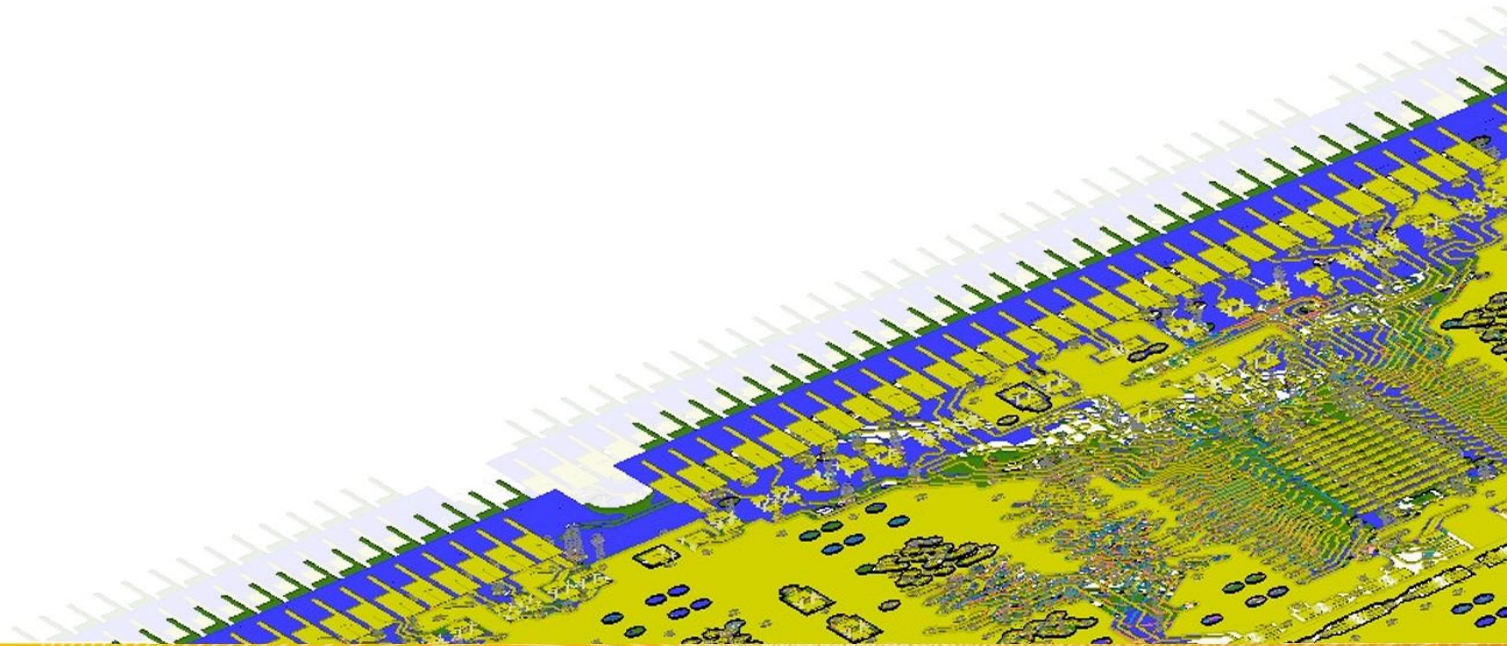




Design Space Exploration for Signal Integrity

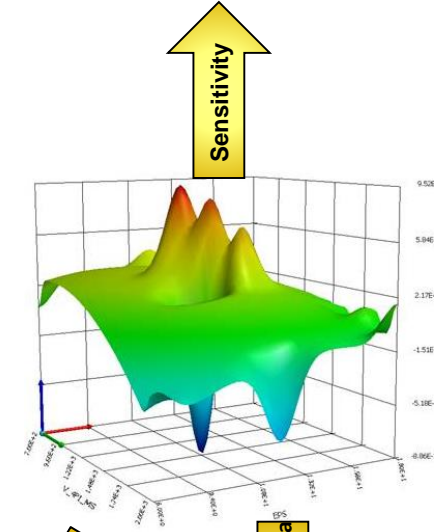
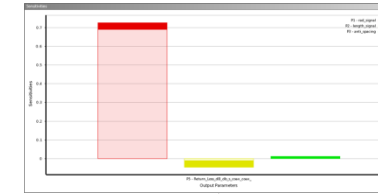


Overview

- **Introduction to Design Space Exploration**
 - Cornerstone Technology
 - DesignXplorer
- **Utilizing Design Space Exploration for Signal Integrity**
 - Pre-layout what-if analysis
 - Post-layout Optimization
 - Manufacture variables study(6 sigma)
- **Full Hardware Utilization for Design Space Exploration**
 - High Performance Computing (HPC)
 - Distributed Solve Option (DSO)
- **Conclusions**

Introduction to Design Space Exploration

- Design Space Exploration is the ability for a user to explore the design space of a structure in simulation space so that they can have a design with optimum performance and manufacturability
- Design Space Exploration is **MORE** than an optimization.
 - A simple optimization is similar to walking a foot path to a desired destination though the forest... The walker knows nothing about the surrounding area away from the path other than they 'seem' to arrived at their destination
- Design Space Exploration is the exploration of a design's performance in the whole design space. Each variable is explored so that there can be many paths to an optimum with much more insight into the sensitivities of output quantities with respect to the design variables.

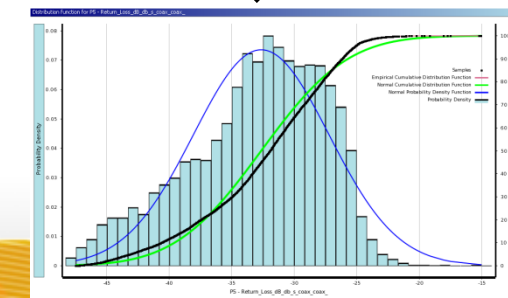


Sensitivity

Optimization

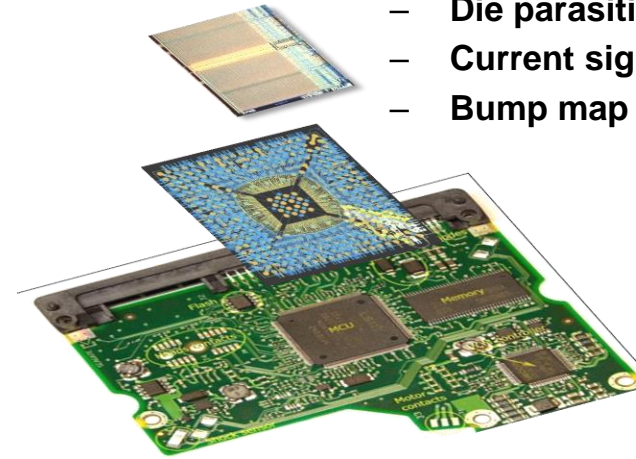
Design for Six Sigma

	A	B	C	D	E	F
1	P1 - ref_signal	P2 - length_upsl	P3 - ant_spacing	P4 - Return_Loss_0.5Hz	P5 - Return_Loss_0.5GHz	
2	Optimization Study					
3	Objective	No Objective	No Objective	No Objective	No Objective	Minimize
4	Target Value					
5	Importance	Default	Default	Default	Default	Higher
6	Design Space					
7	Candidate A	-29.9	-303.6	-40.46	-12	-24.66
8	Candidate B	-29.15	-191.2	-38.93	-12	-33.06
9	Candidate C	-28.80	-190.2	-36.08	-12	-24.7



Why Using Design Space Exploration in SI?

- Electronics is hierarchy, different variable takes different role, those variables combination also displays different effect.
- Signal Integrity's goal is searching a balance design---trade off between performance and cost.



- Chip

- On-chip decoupling
- Die parasitics
- Current signature
- Bump map

- Package

- Plane shapes
- Discretes decoupling
- I/O routing
- Ball map

- PCB

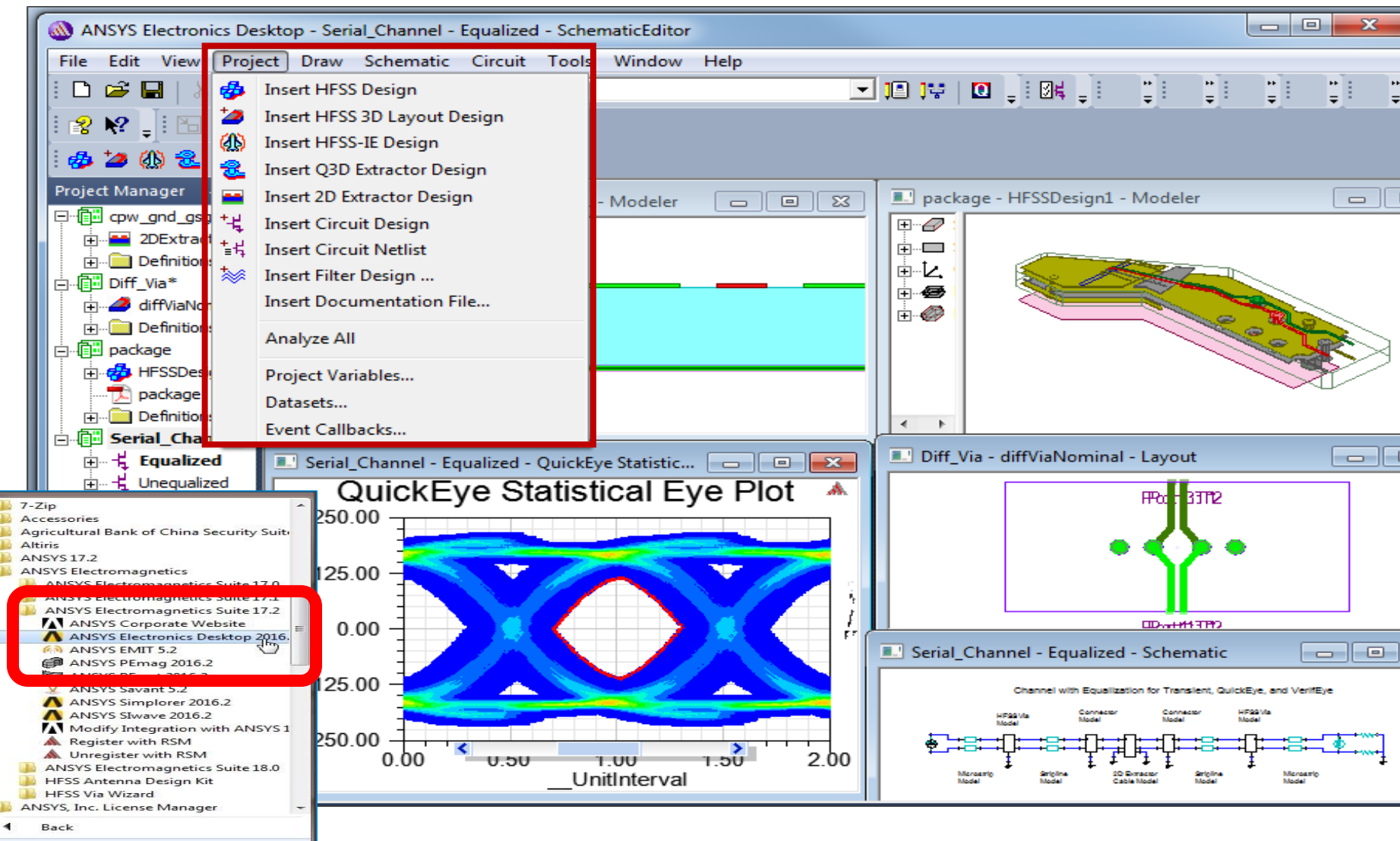
- Channel/SSO Analysis
- Multi-domain
- EMI Due to Current Signature

Dr. Howard Johnson:

"Maximize the performance and minimize the cost of interconnection technology used in high-speed digital designs"

From <http://www.sigcon.com>

ANSYS Electronics Desktop: Integrated platform for SI



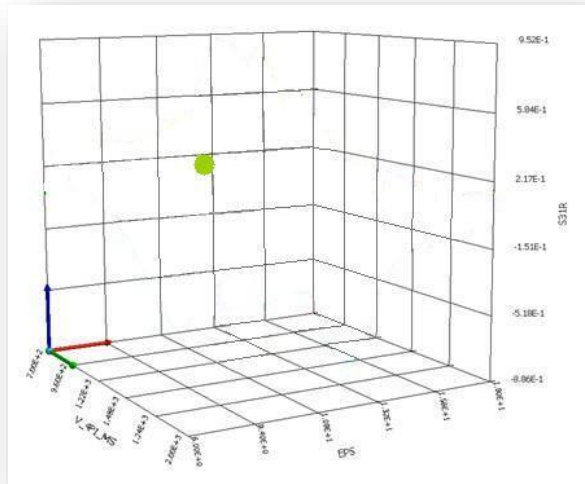
Single Desktop for:

- HFSS
- Q3D
- HFSS 3D Layout
- Planar EM
- Circuit
- System

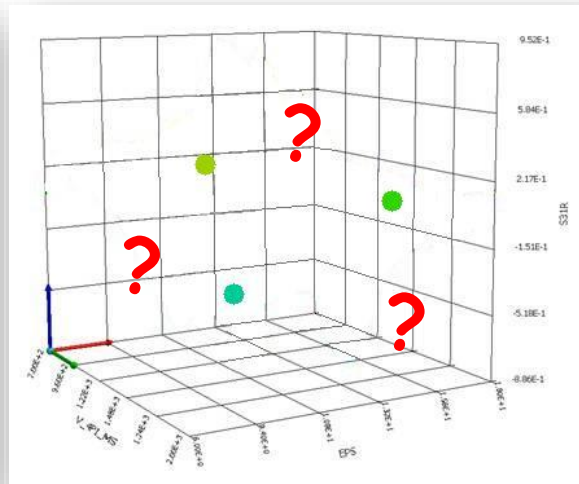
Tight integration between circuit and 3D simulation

What is DesignXplorer?

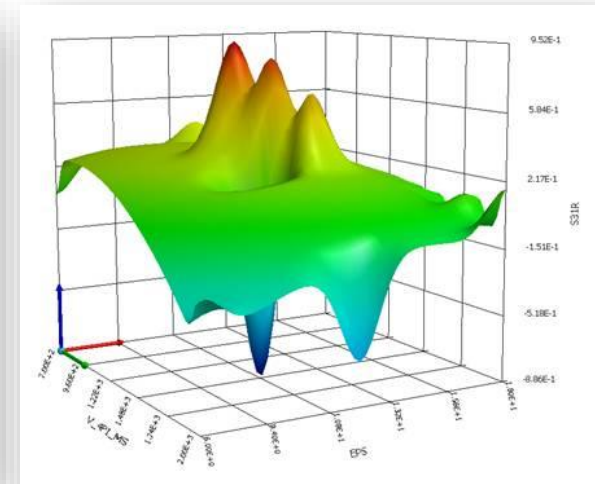
- **DesignXplorer is ANSYS powerful approach to explore, understand and optimize your engineering challenges for ANSYS Multiphysics analysis solvers, including electromagnetic.**
 - Determine the key parameters influencing the design
 - Explore and understand the performance at other design or operating conditions
 - Find the conditions which give the best performance
 - Explore the robustness of the design



Single Point

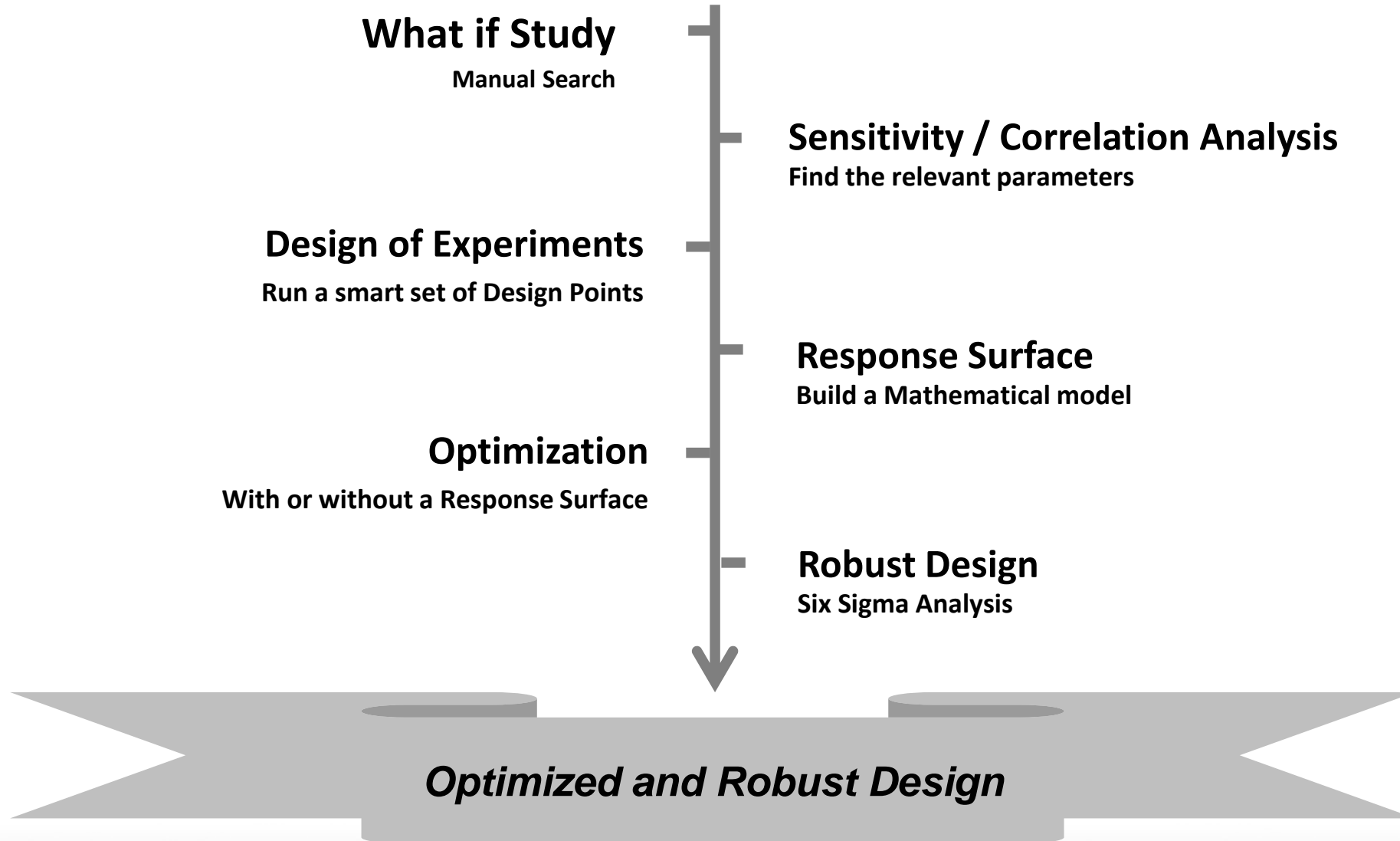


What If?



Response Surface

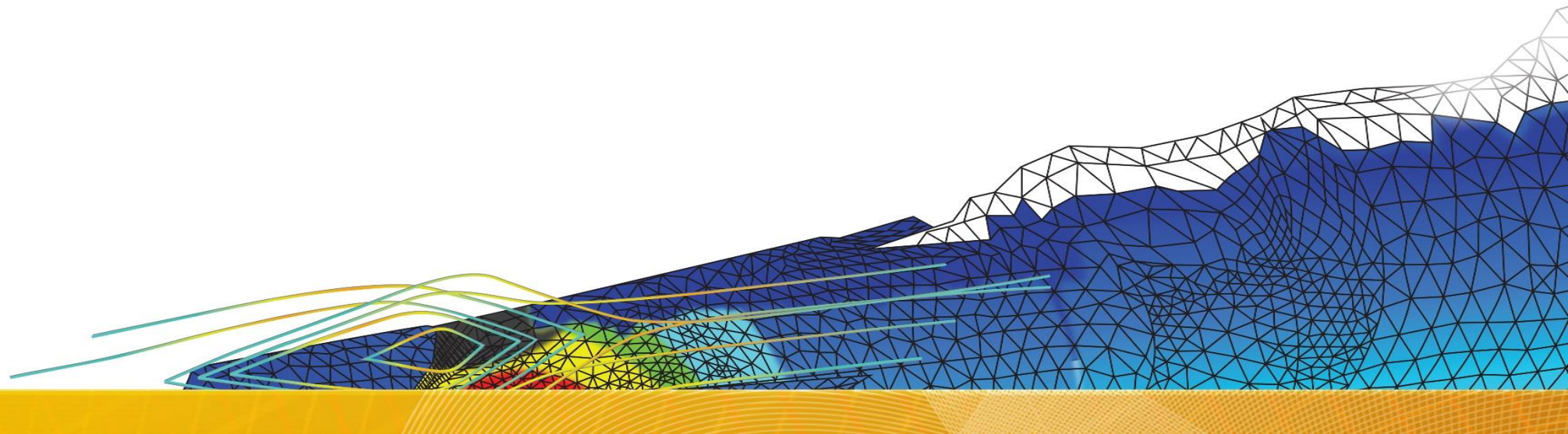
DesignXplorer Features





Utilizing Design Space Exploration for Signal Integrity

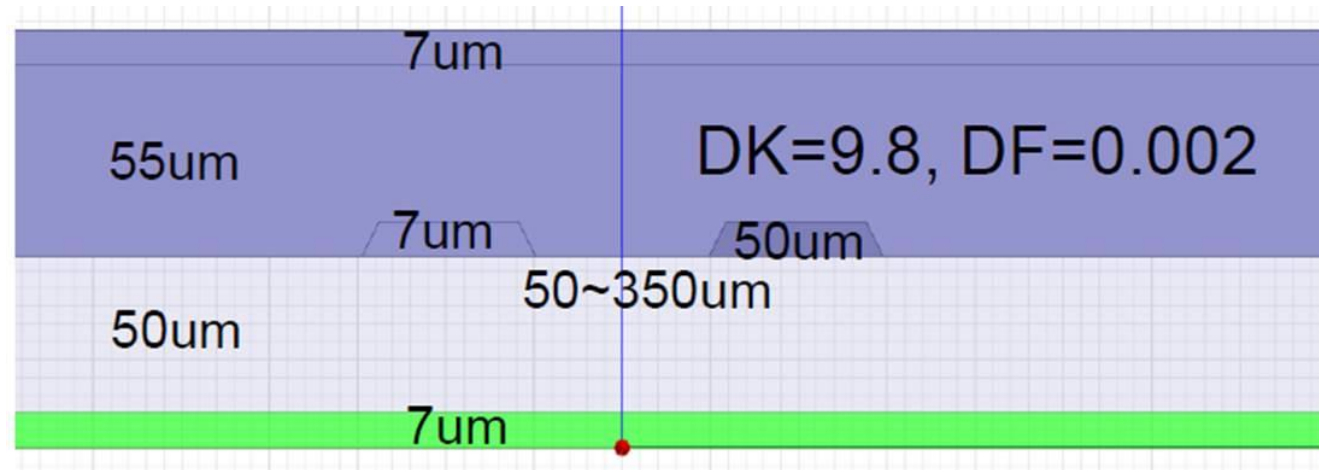
Pre-layout what-if analysis



Pre-layout what-if analysis

- Differential stripline study with DesignXplorer

—



- **Optimization goals**

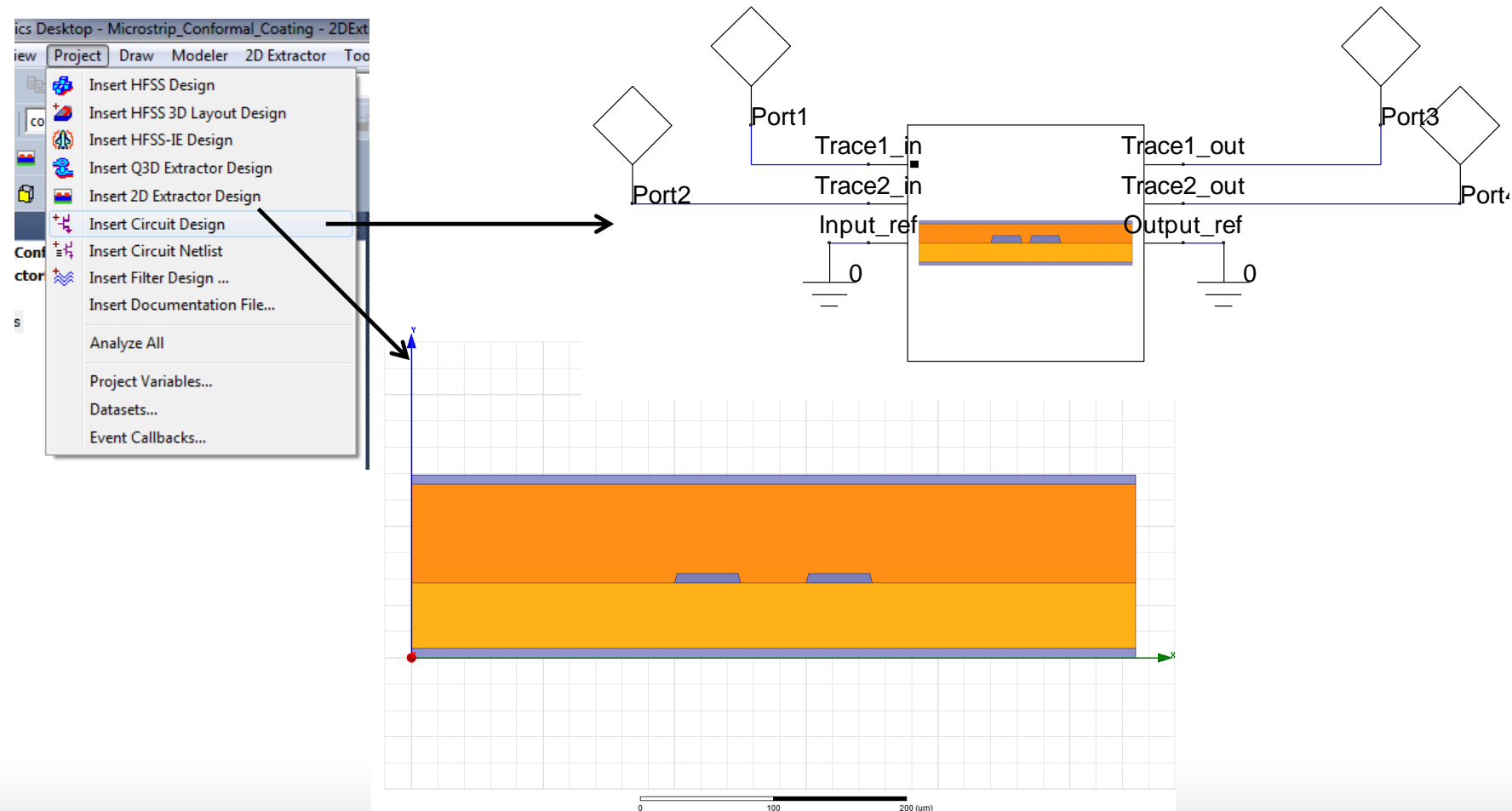
- Characteristic Impedance: Z_0 (differential) $\sim 90\text{ ohm}$
- Minimize Insertion loss: $>-3\text{dB}$
- Maximize Return Loss: $<-10\text{dB}$

- **Optimization variables**

- $DK=8\sim 10$
- $DF=0.0013\sim 0.0024$
- Width= $50\sim 80\mu m$
- Separation= $1W\sim 3W$
- Dielectric Thickness: $50\sim 75\mu m$
- Metal Thickness: $7\sim 19\mu m$
- Metal Conductivity: $0.67E7\sim 1.5E7\text{ Siemens/m}$

Differential stripline model buildup

- Create a ANSYS Electronics Desktop project with Circuit Design in dynamic linked 2D Extractor
 - 2D Extractor design: optimize impedance
 - Circuit Design: optimize insertion loss and return loss



DesignXplorer Response Surface Optimization setup

Project Schematic

1 Q3D 2D Extractor
2 Geometry
3 Setup
4 Solution

2DExtractorDesign1 (Closed)

- 3D Components
- Model
- Boundaries
- Conductors
- Mesh Operations
- Reduce Matrix
- Analysis
- Optimetrics
- DefaultDesignXplorerSetup
- Results
- Field Overlays
- Circuit1
- Data
- Excitation
- Ports
- W113
- Analysis
- Design
- SoD Co
- Optime

DesignXplorer Setup

General | Table | Calculations | Goals | Options

Sim. Setup

Design Variable	Include	Override	Value	Units
\$Bottom_Die_Thick	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	50	um
\$DF	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	0.00174240099658937	
\$DK	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	10	
\$TOP_Die_Thick	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	75	um
\$conductivity	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	6700000	
\$etch_ratio	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	0.5	
\$plane_thickness	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	7	um
\$spacing	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	10	um
\$trace_thickness	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	7	um
\$trace_width	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	20	um

Input Variables

DesignXplorer Setup

General | Table | Calculations | Goals | Options

Calculation

Name	Solution	Calculation
------	----------	-------------

Add/Edit Calculation

Context: Standard
Report Type: LinearFrequency
Domain: Sweep
Show: Differential pairs

Calculation Expression: $dB(S(DIFF1, DIFF1))$

Category: S Parameter
Quantity: S(DIFF1, Comm1)
Function: dB

Set Range Function

Range function: Specified
Category: Math
Function: mean
Purpose: Return mean of given values.

Over sweep: F Range [0.5GHz:1.5GHz]

Optimization Goal

Design of Experiments variable table generation

- Create Design of Experiments variable table
 - Specify design variable range setup
 - Preview the Design of Experiments variable table

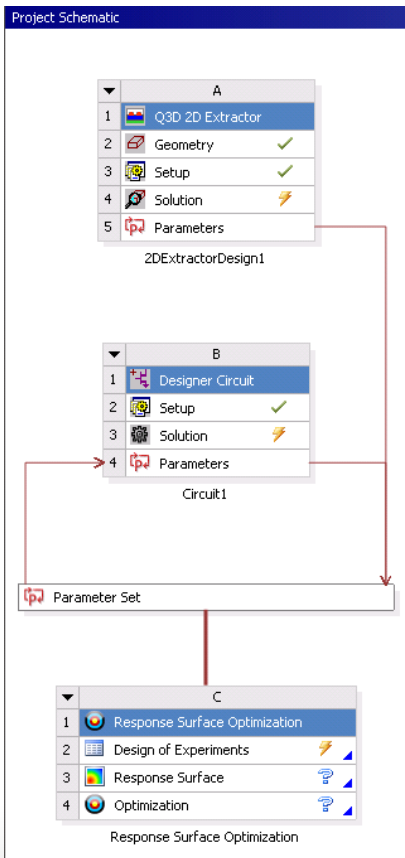


Table of Schematic C2: Design of Experiments

	A	B
Design of Experiments		Enabled
Input Parameters		
Stripline_Differential_Created_April09003550_UTC (B1)		
P10 - \$trace_width [um]		<input checked="" type="checkbox"/>
P11 - \$spacing [um]		<input checked="" type="checkbox"/>
P12 - \$TOP_Die_Thick [um]		<input checked="" type="checkbox"/>
P13 - \$Bottom_Die_Thick [um]		<input checked="" type="checkbox"/>
P14 - \$trace_thickness [um]		<input checked="" type="checkbox"/>
P15 - \$plane_thickness [um]		<input checked="" type="checkbox"/>
P16 - \$conductivity		<input checked="" type="checkbox"/>
P17 - \$etch_ratio		<input checked="" type="checkbox"/>
P18 - \$DK		<input checked="" type="checkbox"/>
P19 - \$DF		<input checked="" type="checkbox"/>
P20 - \$diffspacing [um]		<input checked="" type="checkbox"/>
Output Parameters		
Circuit1 (A1)		
P4 - max(dB(S(Diff1,Diff1)))		
P5 - min(dB(S(Diff1,Diff2)))		
Stripline_Differential_Created_April09003550_UTC (B1)		
P9 - mag(Z0(Pair1:df,Pair1:df))		
Charts		
Parameters Parallel		
Design Points vs Parameter		

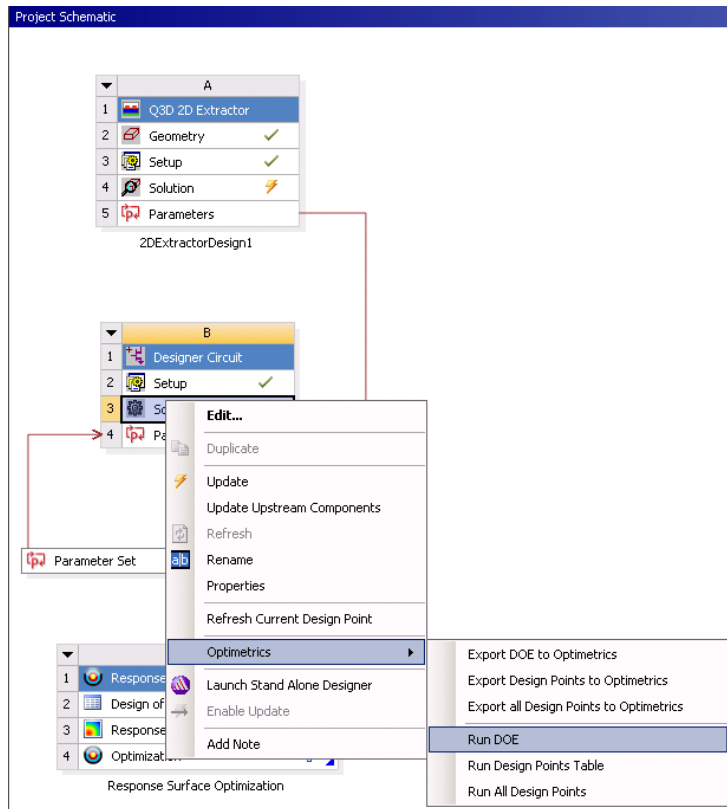
Input variables
Optimization goals

Table of Outline A2: Design Points of Design of Experiments

	A	B	C	D	E	F	G	H	I	J
1	Name	P10 - \$trace_width [um]	P11 - \$spacing [um]	P12 - \$TOP_Die_Thick [um]	P13 - \$Bottom_Die_Thick [um]	P14 - \$trace_thickness [um]	P15 - \$plane_thickness [um]	P16 - \$conductivity	P17 - \$etch_ratio	P18 - \$DK
2	1	21.907	9.5232	71.921	52.781	7.0649	7.1205	6.5225E+06	0.51921	9.3245
3	2	19.152	10.026	80.364	48.609	7.5656	6.3788	7.1615E+06	0.47616	10.212
4	3	21.43	9.947	80.662	47.417	7.0464	7.6397	6.6911E+06	0.49272	9.8543
5	4	19.735	9.7086	74.901	51.722	7.6861	6.9351	6.8775E+06	0.54437	10.901
6	5	19.232	9.1921	75	53.311	7.3152	6.5735	6.1054E+06	0.51258	10.649
7	6	21.695	9.8543	79.669	46.755	7.2596	7.1669	7.3656E+06	0.49669	10.993
8	7	19.523	10.185	76.291	51.391	7.4821	6.6848	6.0433E+06	0.52715	10.384
9	8	20.265	10.013	77.682	49.801	6.5457	6.5272	6.4693E+06	0.45762	9.0728
10	9	18.517	9.8808	79.768	48.808	6.351	6.6384	6.7799E+06	0.46225	9.8675
11	10	18.331	9.5629	77.185	45.298	6.5364	6.9444	6.8952E+06	0.46954	10.861
12	11	21.642	9.245	71.523	51.788	6.3139	6.5921	7.0372E+06	0.50861	10.464
13	12	18.305	10.954	77.881	48.013	6.7497	7.1082E+06	0.48477	0.48477	9.6291
14	13	18.172	10.702	69.04	48.742	7.5748	6.7868	6.7976E+06	0.51722	9.1921
15	14	21.325	10.596	80.066	47.815	6.4252	7.4914	7.2058E+06	0.52848	10.172
16	15	18.781	9.8013	70.828	52.583	6.8609	7.6954	7.197E+06	0.47682	9.7086
17	16	20.954	9.9868	81.755	48.278	7.0834	7.204	6.345E+06	0.53974	9.5497
18	17	19.285	9.6954	72.914	52.45	7	6.4715	6.1143E+06	0.54834	9.9073
19	18	20.053	9.2053	69.636	53.179	7.1762	7.6212	6.7532E+06	0.50331	9.6159
20	19	18.199	10.212	76.887	53.51	6.7868	7.1576	6.4604E+06	0.54702	10.874
21	20	18.146	10.755	78.477	52.053	7.2318	6.6755	7.3034E+06	0.49536	10.702
22	21	20.026	9.7483	78.974	52.318	6.6384	6.8053	7.2946E+06	0.4894	10.821
23	22	20.583	10.583	76.788	54.172	6.5179	7.0278	7.0461E+06	0.50662	9.457
24	23	21.722	9.3775	69.238	53.576	7.0185	7.0464	6.3273E+06	0.49007	10.596
25	24	19.411	10.690	78.170	49.317	6.667	7.6676	6.5035E+06	0.49771	9.4967

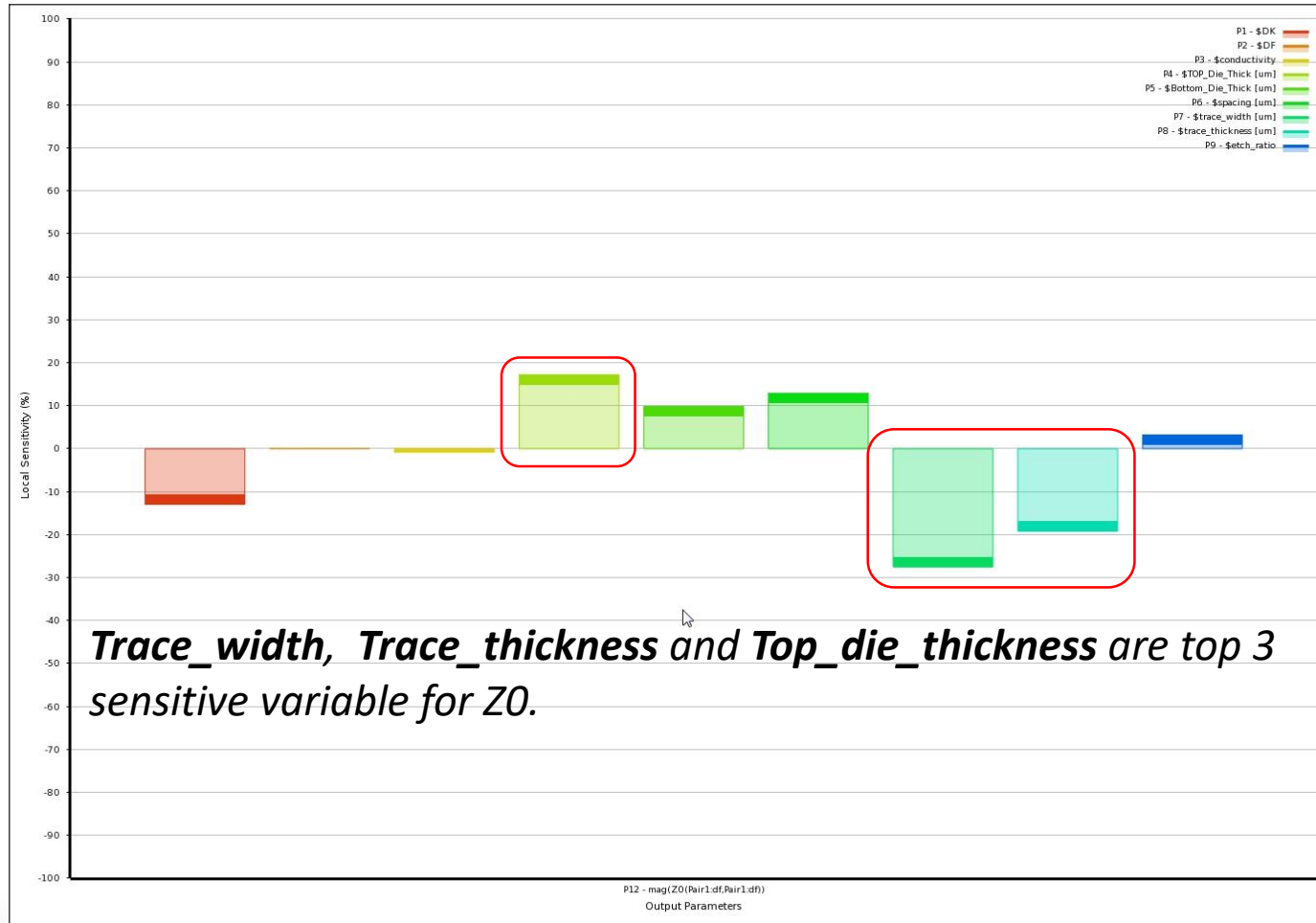
Solve DoE table

- Once the Design of Experiments table is generated, run variable sweeping.
- DSO(Distribution Simulation Option) will distribute variables to multiple nodes to solve simultaneously.

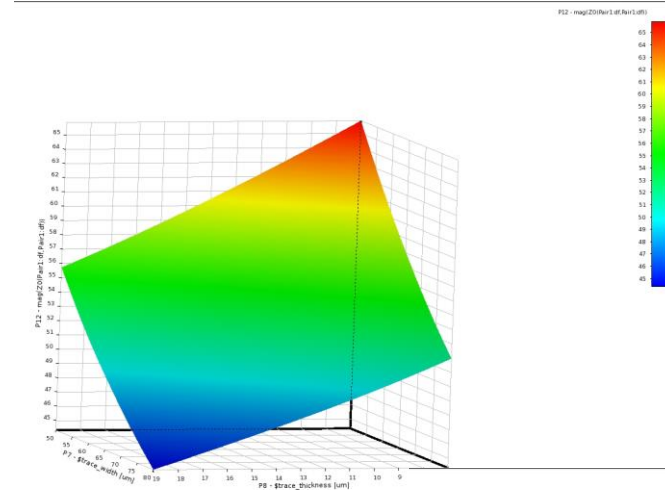


Sensitivity and Response Surface Plots

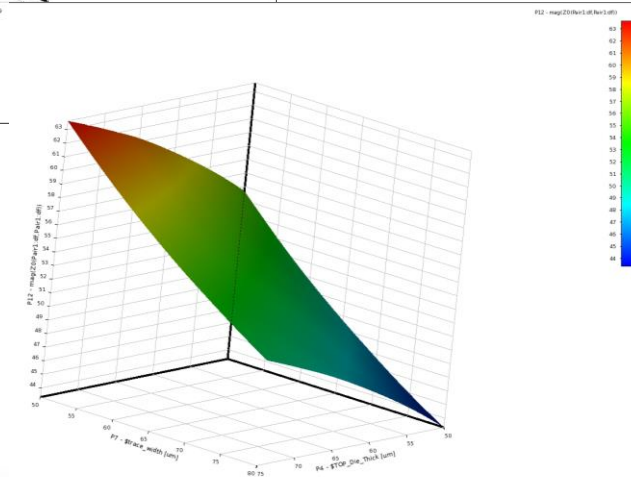
- **Creating Sensitivity and Response Surface for the Design of Experiments results**
 - Sensitivity will display the 2D sensitivity histogram of each input variables vers. output(Z_0).
 - Response displays 3D interaction between variables vers. output (Z_0).



Trace_width, Trace_thickness vs. Z_0



Trace_width, Top_die_thickness vs. Z_0



Optimizing over the Response Surface

- Specify the optimization objectives and constraints
 - Differential Characteristic impedance of 90 ohm with lower bound 85 ohm and upper bound 95 ohm
 - Maximum insertion loss
 - Minimum Return Loss

	A	B	C	D	E	F	G
1	Name	Parameter	Objective		Constraint		
2			Type	Target	Type	Lower Bound	Upper Bound
3	Seek P9 = 90; 85 <= P9 <= 95	P9 - mag(Z0(Pair 1:df,Pair 1:df))	Seek Target	90	Lower Bound <= Values <= Upper Bound	85	95
4	Maximize P4	P4 - max(dB(S(Diff1,Diff1)))	Maximize		No Constraint		
5	Minimize P5	P5 - min(dB(S(Diff1,Diff2)))	Minimize		No Constraint		
*		Select a Parameter					

- The best benefit of the Response Surface approach in DesignXplorer is that the user can change the values of the cost and re-optimize with no further explicit simulations

	A	B	C	D	E	F	G	H	I	J	K
1	Reference	Name	P10 - \$trace_width [um]	P11 - \$spacing [um]	P12 - \$trace_thickness [um]	P4 - max(dB(S(Diff1,Diff1)))	P5 - min(dB(S(Diff1,Diff2)))	P9 - mag(Z0(Pair 1:df,Pair 1:df))			
2						Parameter Value	Variation from Reference	Parameter Value	Variation from Reference	Parameter Value	Variation from Reference
3		Candidate Point 1	18.027	85.596	7.1925	★ -6.3503	0.00 %	✗ -5.4534	0.00 %	★ 90.202	0.00 %
4				87.379	7.4801	★ -6.3831	-0.52 %	✗ -5.4322	0.39 %	★ 90.055	-0.16 %
5				91.924	7.4799	★ -6.472	-1.92 %	✗ -5.4625	-0.17 %	★ 90.596	0.44 %
30				19		-6.2803		-3.5846			

Explore Response Surface at Point
 Insert as Design Point
 Insert as Refinement Point
 Insert as Verification Point
 Insert as Custom Candidate Point
 Verify by Design Point Update
 Export Data

Candidate Point 1
 Candidate Point 2
 Candidate Point 3

Final Optimized results

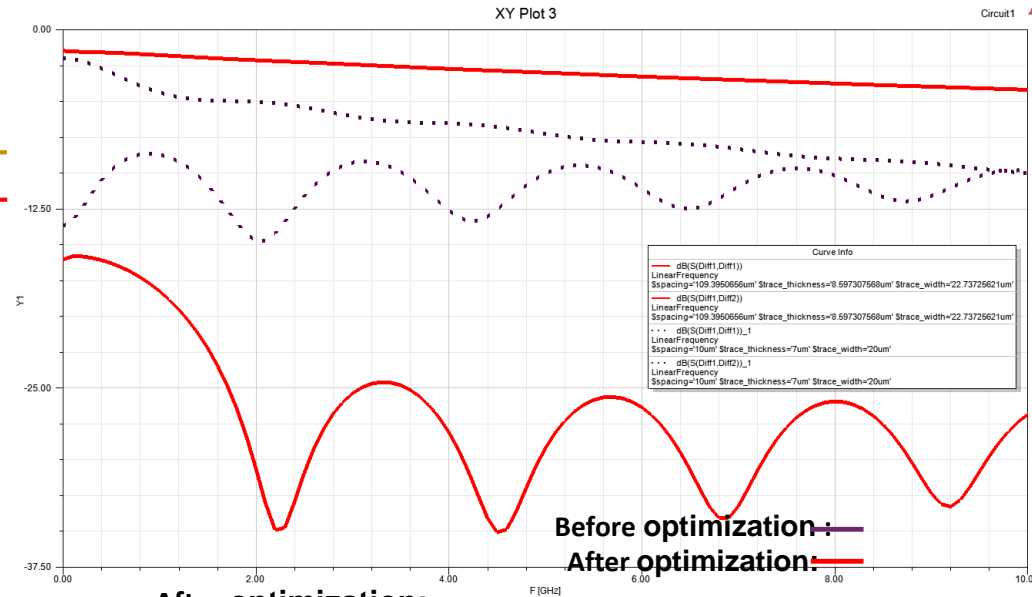
- After you verify the candidate points, choose the best one for the design

— IL&RL:

- Before optimization: Gray dot line
- After optimization: Red solid line

— Differential Character Impedance:

- Before optimization: 49.5ohm
- After optimization: 84.3 ohm



Before optimization

Simulation: Setup1 LastAdaptive

Design Variation: topdielectricthickness='75um' toptracewidth='16.5um' tracespacin

Profile | Convergence | Matrix | Tline Data | Mode Data | Mesh Statistics

View Options... 10 (GHz)

DiffPairMatrix1 All Freqs

	Z0:Pair1:cm (ohm, ohm)	Z0:Pair1:df
Freq: 10 (GHz)		
Pair1:cm	(32.851,-0.95596)	(-0.0019657,-0.0010077)
Pair1:df	(-0.0019657,-0.0010077)	(49.554,-3.5783)

After optimization:

View Options... 10 (GHz)

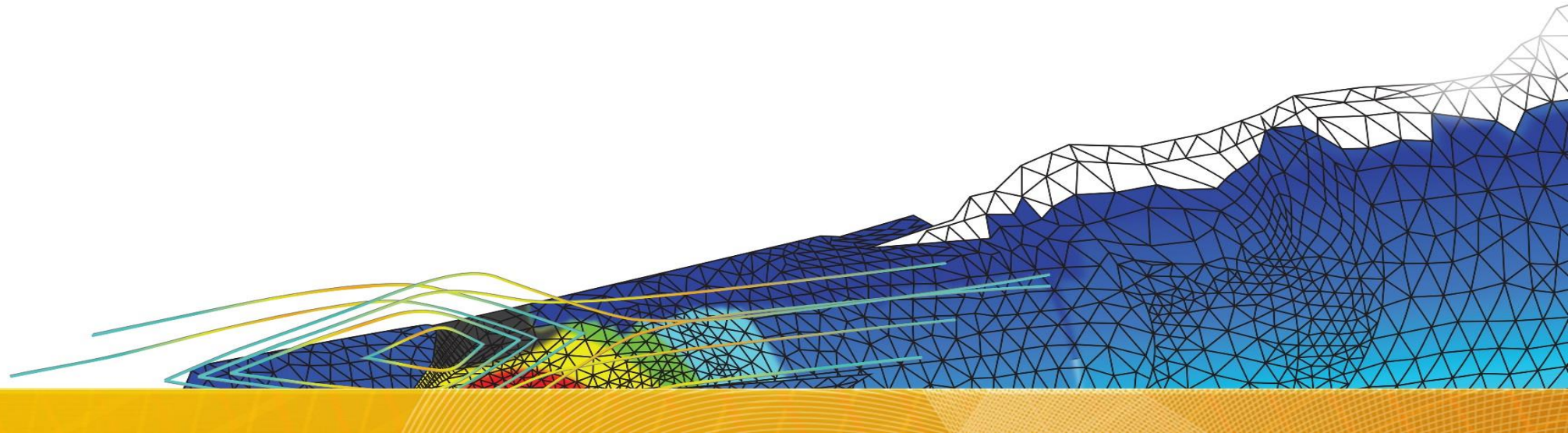
DiffPairMatrix1 All Freqs

	Z0:Pair1:cm (ohm, ohm)	Z0:Pair1:df
Freq: 10 (GHz)		
Pair1:cm	(22.497,-0.74386)	(-0.00039257,-0.0019157)
Pair1:df	(-0.00039257,-0.0019157)	(84.38,-2.8461)

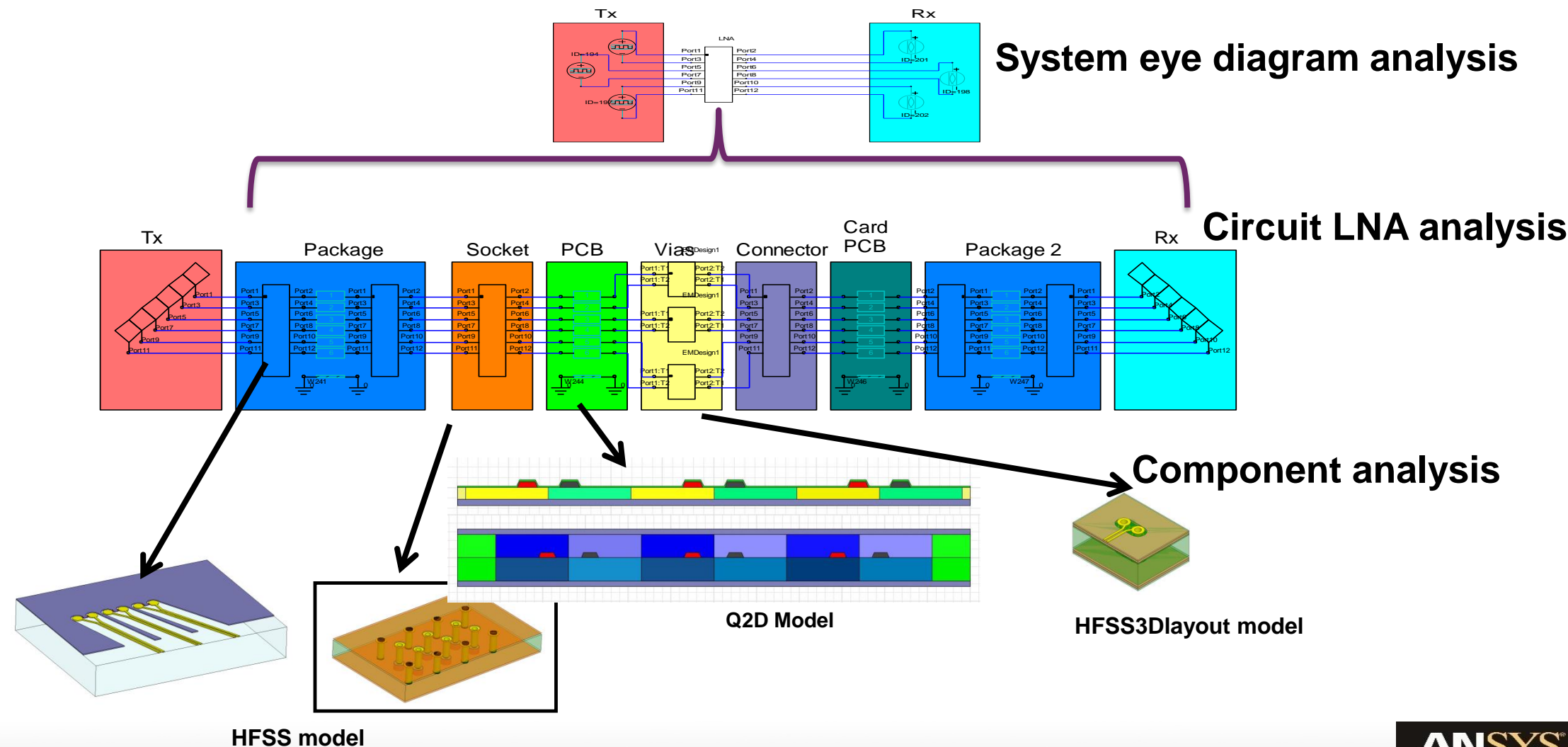


Utilizing Design Space Exploration for Signal Integrity

Post-layout Optimization



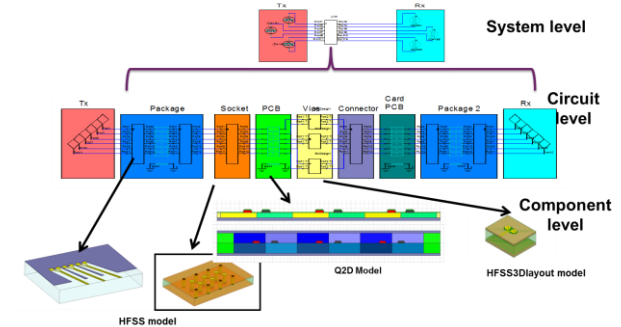
Hierarchy PCIe Channel Example



PCIe Serial Channel Design Problem Scale

30 different factors are unreasonable considering an entire PCIe Channel, for example:

- Package
 - Thickness, Pad breakout, trace length, ball pitch, dielectric material (5)
- Socket
 - Thickness, material properties, SG via ratio (3)
- Board
 - MS and SL trace & space, etch factors, Cu roughness, dielectric materials, via config (8)
- Connector
 - Various vendor models, often only one or two options. (1)
- 2nd Board
 - MS, SL, etch factors, Cu roughness, dielectric materials, via config (8)
- 2nd Package
 - Thickness, Pad breakout, trace length, ball pitch, dielectric material (5)

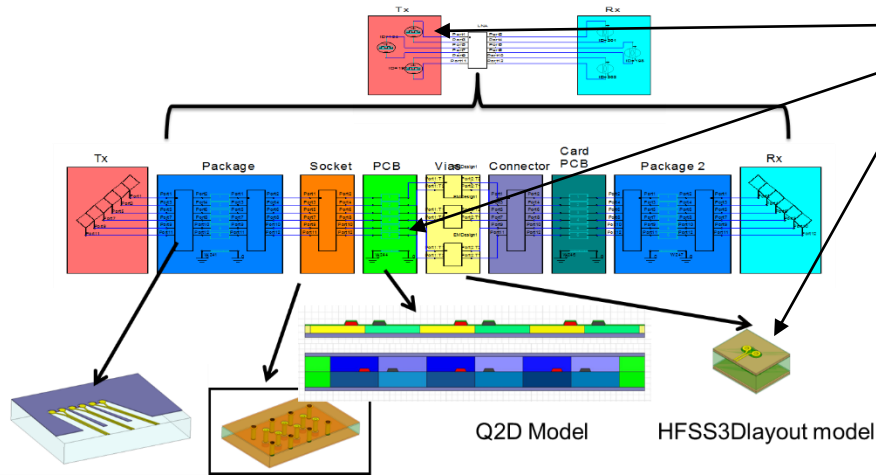


If each factor has 4 variable value, the total combination scenario will be 120

Different level variables combination affect different level character

• Sweeping variables

- \$FFE/DFE level on **System** level (Discrete distribution)
- \$PCB_trace_length on **Circuit** level (Continues distribution)
- \$anti_pad on **Component** level (Continues distribution)



Properties: DOE_eye_Hierarchy

Project Variables | Intrinsic Variables | Constants

Value Optimization Tuning Sensitivity Statistics

Name	Value	Unit	Evaluated Value	Description	Read-only	Hidden	Sweep
\$Package_trace_length	0.01	meter	0.01meter		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$Socket_Array_Index	0		0		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$PCB_Array_Index	0		0		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$Via_Model_Array_Index	0		0		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$Card_trace_length	0.01	meter	0.01meter		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$FFE_TAP	2		2		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$PCB_Trace_Length	0.05	meter	0.05meter		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$antiPad	770	um	770um	Signal via antipad diam...	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$GND_Via_Pad	30	mil	30mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$GND_Via_Antipad	25	mil	25mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$GND_Via_Drill	12	mil	12mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$Sig_Via_Pad	20	mil	20mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$Sig_Via_Antipad	10	mil	10mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$Sig_Via_Drill	8	mil	8mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$SM_Top	0.9	mil	0.9mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$L1_THK	0.7	mil	0.7mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$D1_THK	4	mil	4mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$L2_THK	0.7	mil	0.7mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$D2_THK	4	mil	4mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$L3_THK	0.7	mil	0.7mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$D3_THK	4	mil	4mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$L4_THK	0.7	mil	0.7mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$D4_THK	4	mil	4mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$L5_THK	0.7	mil	0.7mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$D5_THK	4	mil	4mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$L6_THK	0.7	mil	0.7mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$D6_THK	4	mil	4mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$L7_THK	0.7	mil	0.7mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$D7_THK	4	mil	4mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$L8_THK	0.7	mil	0.7mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$SMB_THK	0.9	mil	0.9mil		<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
\$Socket_Array	["\$PROJECTDIR\Socket\Socket_1_6_SG...		["\$PROJECTDI...		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
\$PCB_Array	["Diff_SL_76_0hm_20mil_Spacing", "Diff_S...		["Diff_SL_76_O...		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
\$Via_Model_Array	["\$PROJECTDIR\Via_Models\Via_L14_0_...		["\$PROJECTDI...		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

• Optimization goal:

- BER for statistic analysis
- Eye width/height for statistic/circuit analysis(timing domain)
- Insertion loss/Return loss for circuit analysis(frequency domain)

11	P9 - \$Sig_via_Antipad [mil]	
12	Output Parameters	
13	QuickEYE (B1)	
14	P13 - MinEyeWidth(AEYEPROBE(Eye2), 1ns, 0ns, 0ns, 1, 0mV, 1, 0ns)	
15	P14 - MinEyeHeight(AEYEPROBE(Eye2), 1ns, 0ns, 0ns, 1, 0mV, 1, 0ns)	
16	P15 - XWidthAtYVal(AEYEPROBE(Eye2), 1e-012)	
17	LNA (A1)	
18	P10 - min(dB(S(Diff1,Diff2)))	

PCIe Channel DoE data table

Outline of Schematic D2: Design of Experiments

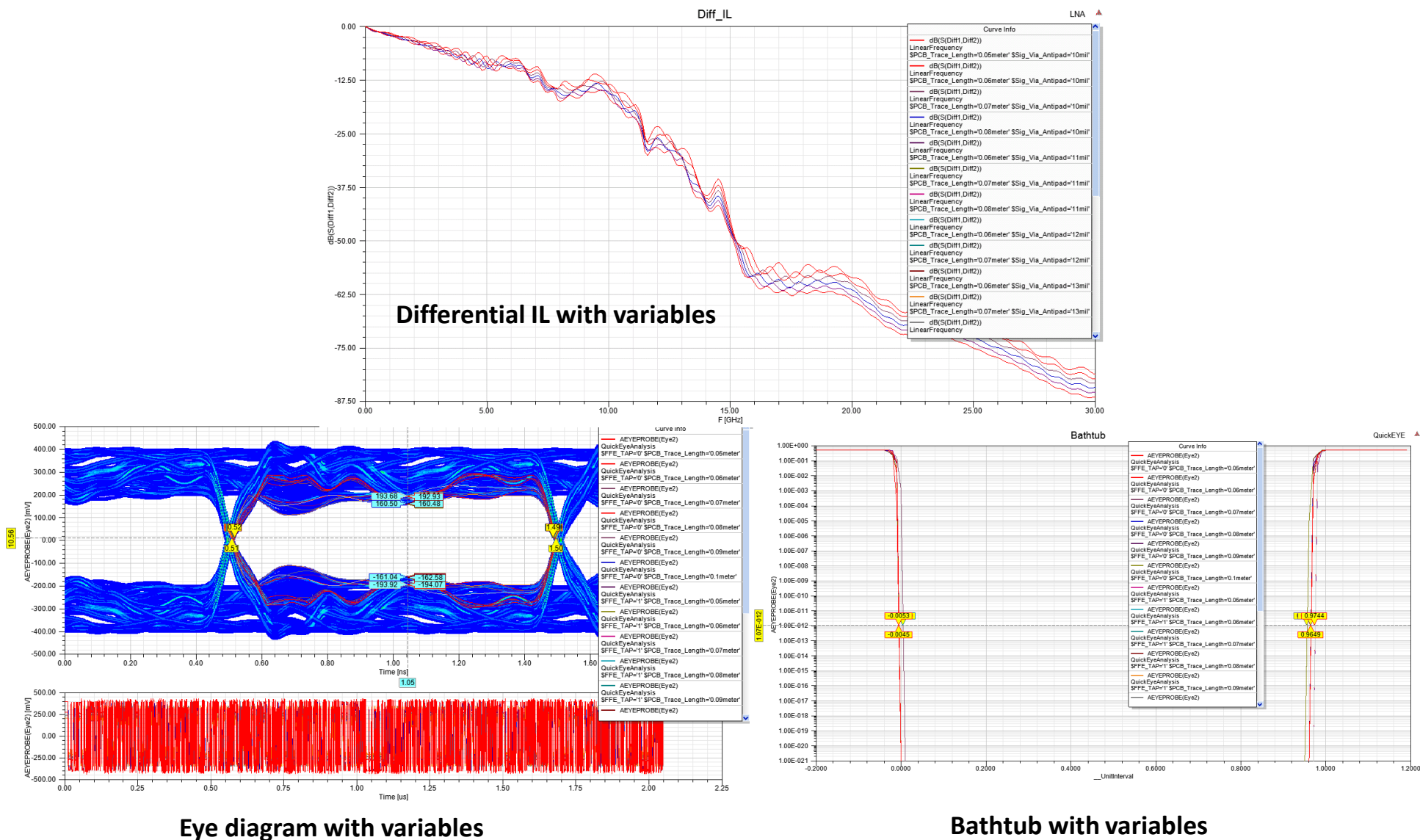
Table of Schematic D2: Design of Experiments (Optimal Space-Filling Design : Max-Min Distance : Maximum Number Of Cycles = 10 : CCD Samples : Random Generator Seed = 0)

Properties of Outline A7: P3 - \$PCB_Trace_Length [meter]

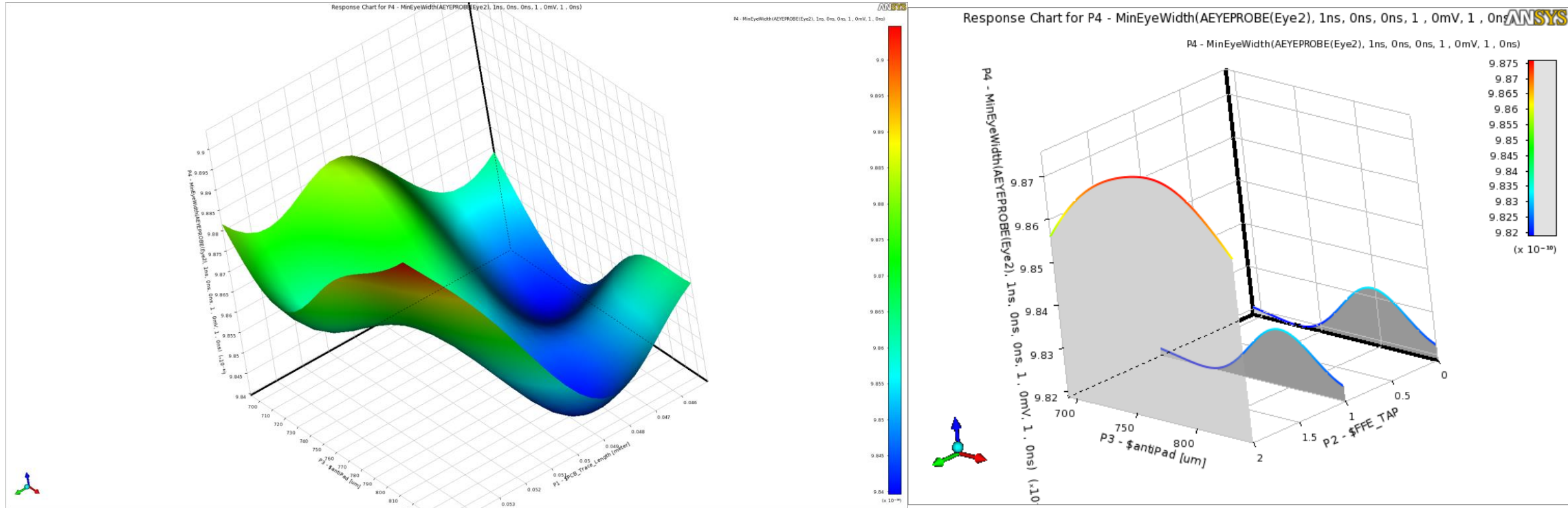
Simplified variable combination scenarios to 50

	A	B	C	D	E	F	G
	Name	P1 - \$FFE_TAP	P12 - \$Sig_Via_Antipad [mil]	P3 - \$PCB_Trace_Length [meter]	P7 - \$PCB_Trace_Length [meter]	P8 - \$FFE_TAP	P9 - \$Sig_Via_Antipad [mil]
1	2	0	13	0.054	0.053	0	12.52
2	3	0	15.64	0.0536	0.071	0	13.24
3	4	0	12.76	0.0464	0.093	0	11.56
4	5	0	13.24	0.0548	0.081	0	11.8
5	6	0	10.84	0.0492	0.067	0	15.4
6	7	DP 1	13.48	0.05	0.051	0	14.92
7	8	0	14.44	0.0532	0.097	0	14.2
8	9	0	15.4	0.0476	0.079	0	11.08
9	10	0	15.88	0.0484	0.065	0	14.44
10	11	0	12.04	0.0508	0.099	0	13
11	12	0	11.08	0.0496	0.059	0	10.36
12	13	0	14.2	0.0524	0.073	0	15.88
13	14	0	13.96	0.0472	0.057	0	12.04
14	15	0	15.16	0.048	0.095	0	13.96
15	16	0	11.8	0.0544	0.077	0	15.16
16	17	0	10.12	0.0528	0.085	0	12.28
17	18	0	14.68	0.0512	0.061	0	10.6
18	19	0	14.92	0.0516	0.091	0	10.84
19	20	0	10.6	0.052	0.063	0	11.32
20	21	0	10.36	0.0468	0.087	0	12.76
21	22	0	12.28	0.0504	0.083	0	13.48
22	23	0	15.4	0.0476	0.079	0	10.12
23	24	0	11.56	0.046	0.089	0	15.64
24	25	0	13.72	0.0452	0.055	0	13.72
25	26	1	13	0.054	0.075	0	14.68
26	27	1	15.64	0.0536	0.053	0	12.52
27	28	1	12.76	0.0464	0.071	0	13.24
28	29	1	13.24	0.0548	0.093	0	11.56
29	30	1	10.84	0.0492	0.081	0	11.8
30	31	DP 2	13.48	0.05	0.067	0	15.4
31	32	1	14.44	0.0532	0.051	0	14.92
32	33	1	15.4	0.0476	0.097	0	14.2
33	34	1	15.88	0.0484	0.079	0	11.08
34	35	1	12.04	0.0508	0.065	0	14.44
35	36	1	11.08	0.0496	0.099	0	13
36	37	1	14.2	0.0524	0.059	0	10.36
37	38	1	13.96	0.0472	0.073	0	15.88
38	39	1	15.16	0.048	0.057	0	12.04
39	40	1	11.8	0.0544	0.095	0	13.96
40	41	1	10.12	0.0528	0.077	0	15.16
41	42	1	14.68	0.0512	0.085	0	12.28
42	43	1	14.92	0.0516	0.085	0	10.6
43	44	1	14.2	0.0516	0.091	0	10.84
44	45	1	11.32	0.0456	0.069	0	11.32
45	46	1	10.6	0.052	0.063	0	12.76
46	47	1	10.36	0.0468	0.087	0	13.48
47	48	1	12.28	0.0504	0.083	0	10.12

PCIe Channel Example – View the swept output

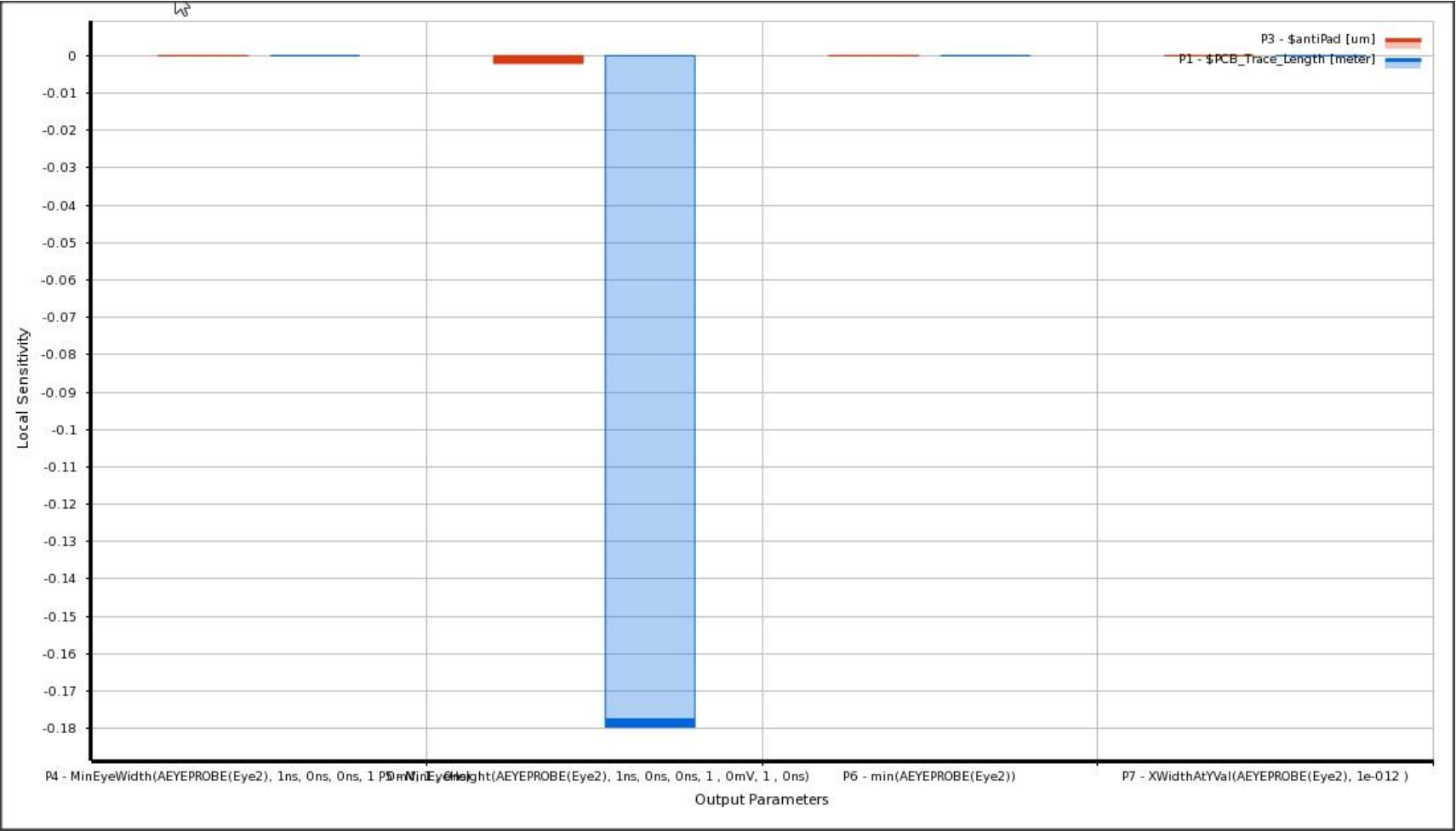


Response Surfaces



- Visualize response surfaces in 3D or 2D plots (continuous, discrete, mixed) variables
- The Measure of fit provides a metric for evaluating the accuracy of the response surface model.
- 3D: *Eye Width* vs. *PCB tracelength & antipad size* / *Eye Width* vs. *FFE & Antipad size*

Sensitivity Plots

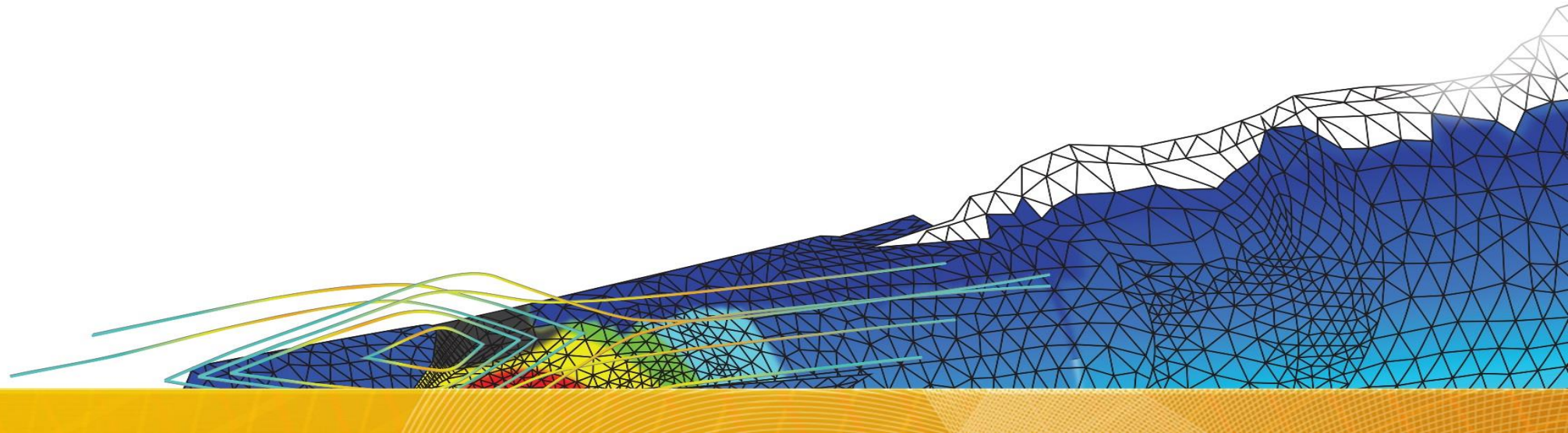


Sensitivity histogram shows that ***\$Trace_length*** is the most sensitive parameter for ***Eye_width***



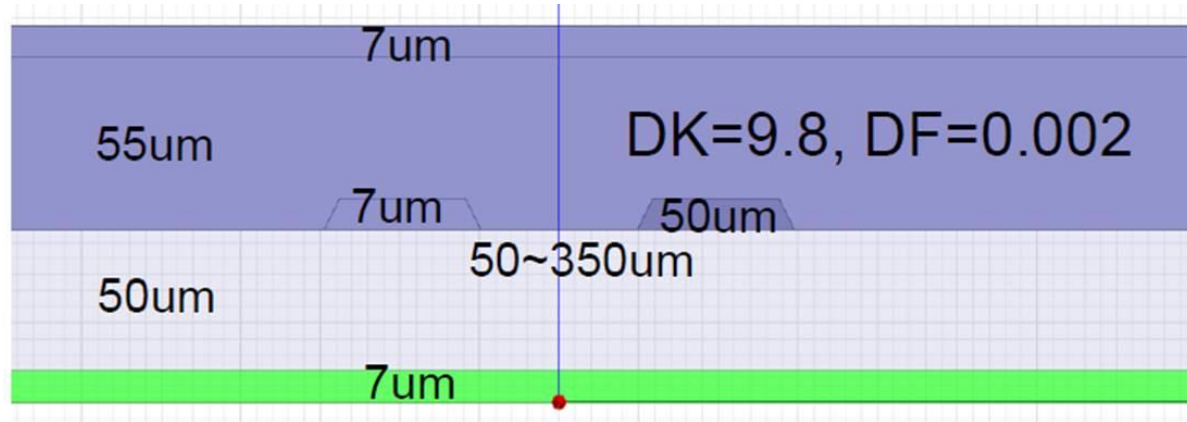
Utilizing Design Space Exploration for Signal Integrity

Manufacture tolerance study (6 σ -six sigma)



DesignXplorer for PCB manufacture tolerance study example

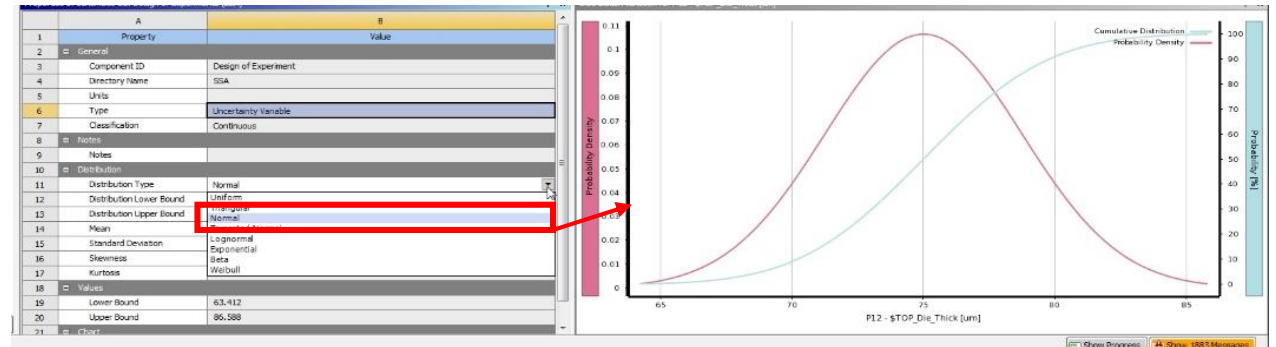
- **Differential stripline study with DesignXplorer**
 - 6σ analysis will be done based on user defined variable range and distribution



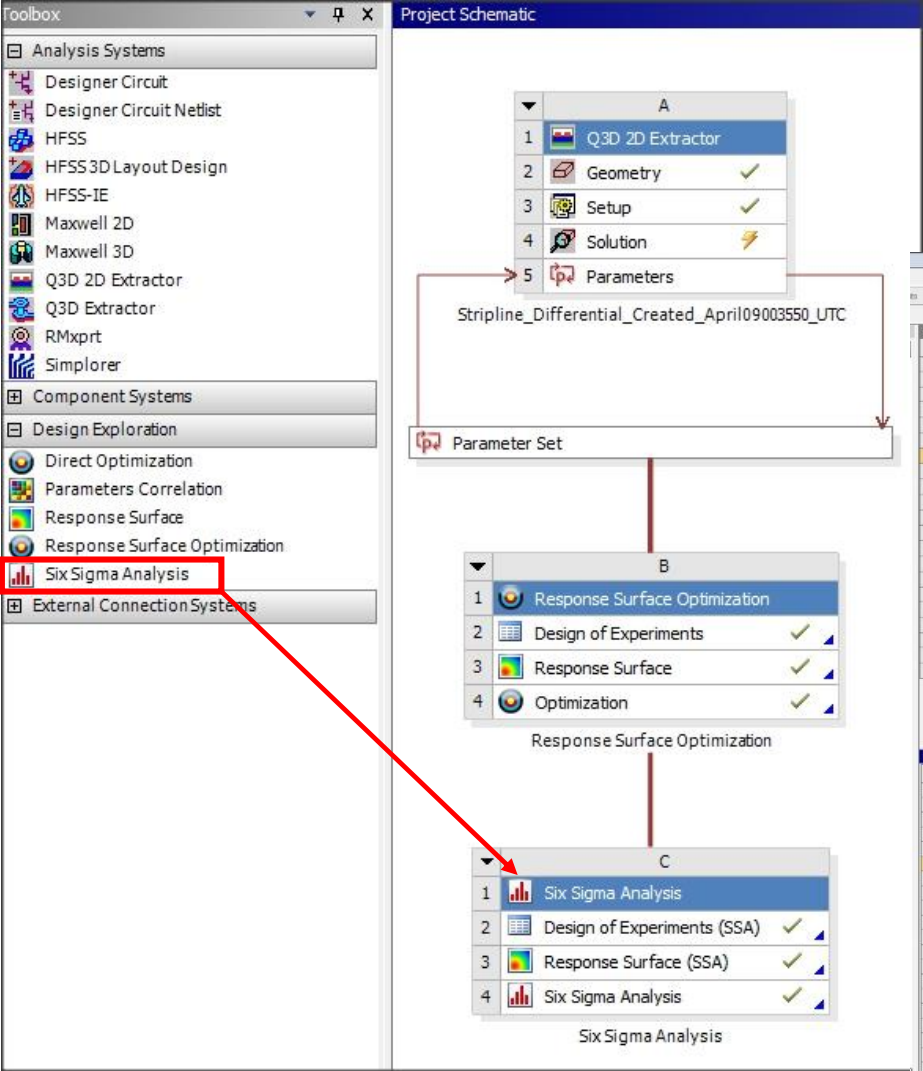
- **Manufacture variables**

- DK=8~10
- DF=0.0013~0.0024
- Width=50~80um
- Separation=1W~3W
- Dielectric Thickness: 50~75um
- Metal Thickness: 7~19um
- Metal Conductivity: 0.67E7~1.5E7 Siemens/m

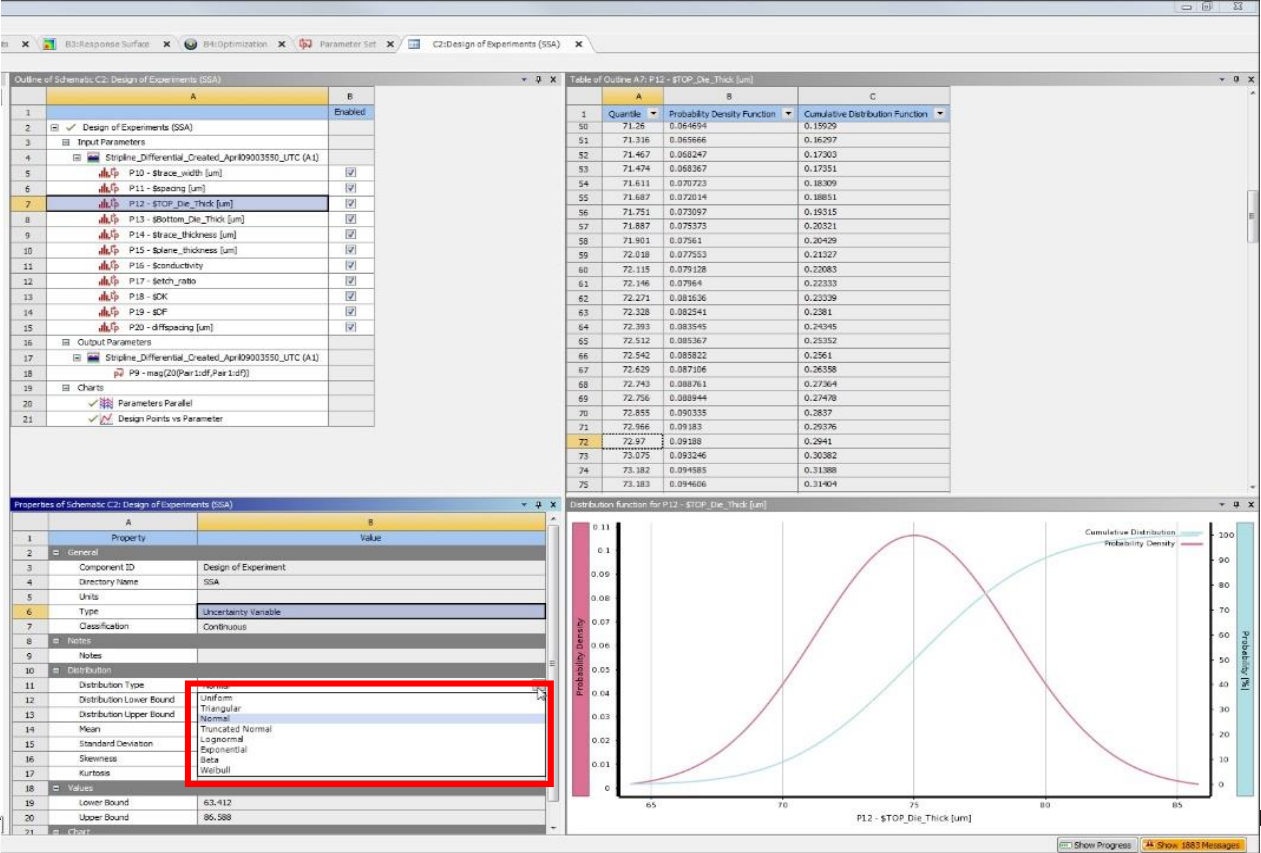
All variables are Normal (Gaussian) distribution



6σ Analysis

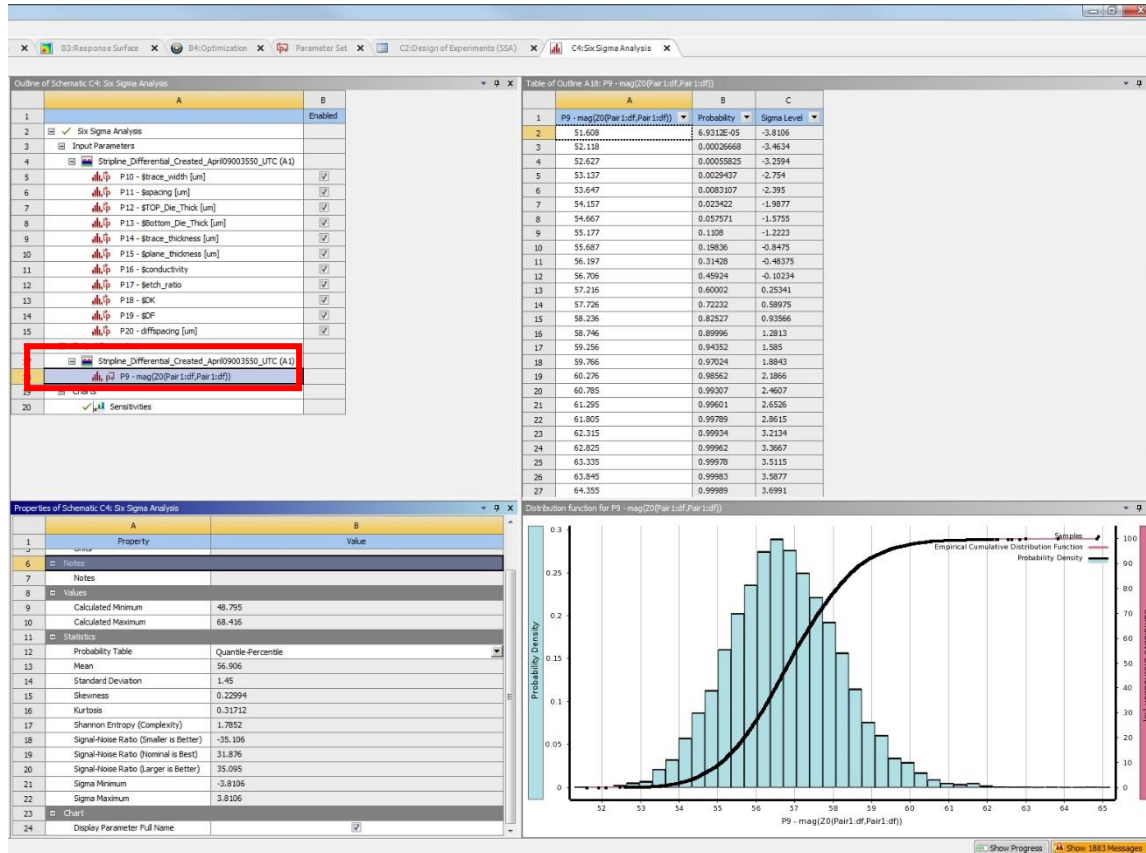


6σ analysis is continuously studying, specifying each variable bounder and distribution.



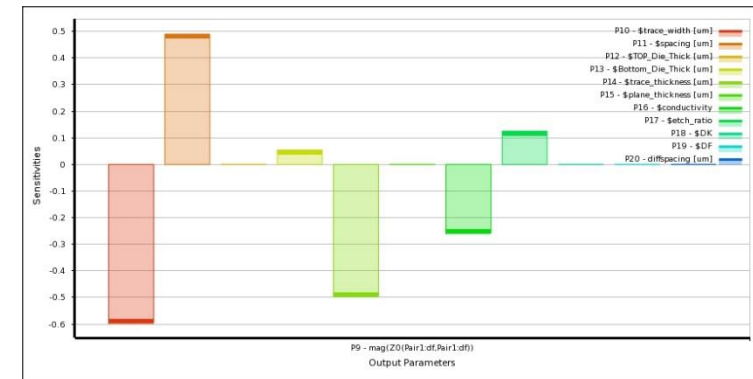
6 σ Analysis results

- 6 σ analysis will give statically distribution function and relative sensitivity curve.



The mean value was 48.79 ohm, peak value was 51.31ohm(min) and 68.47ohm(max)

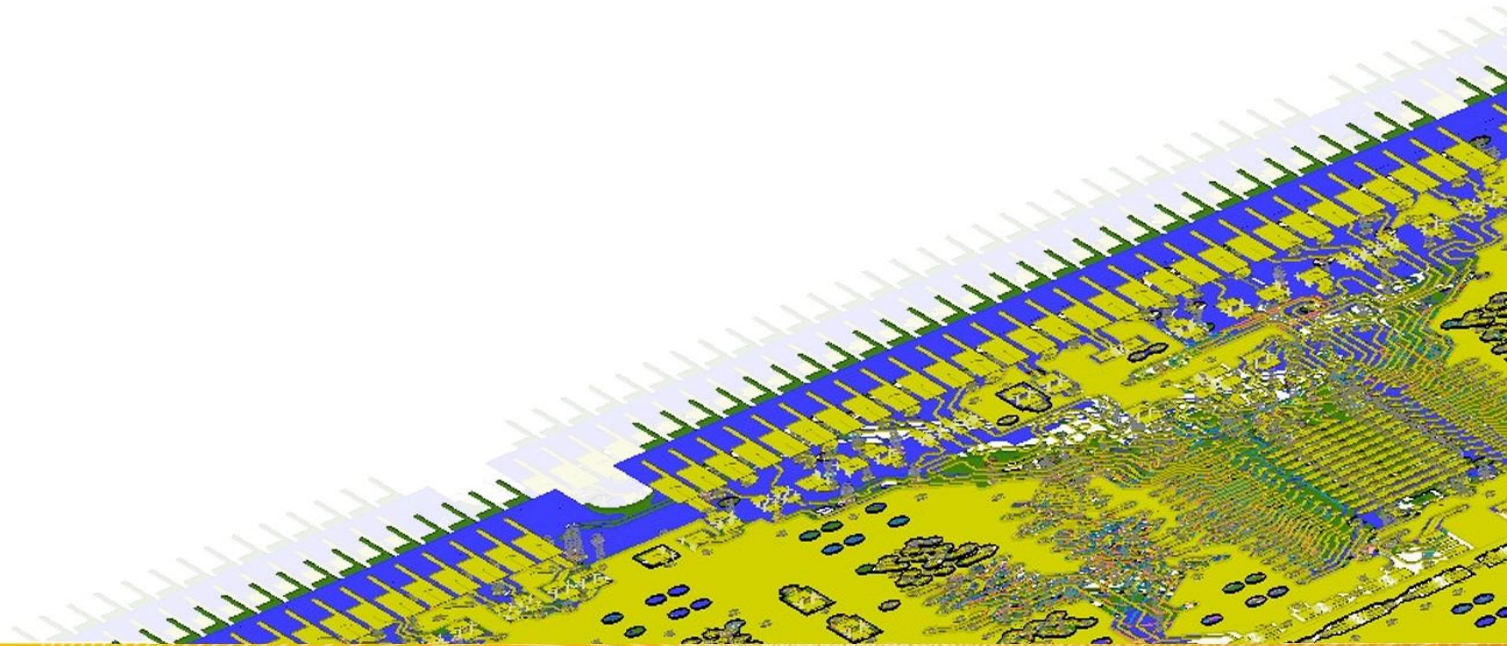
Probability density distribution



Relative Sensitivity results

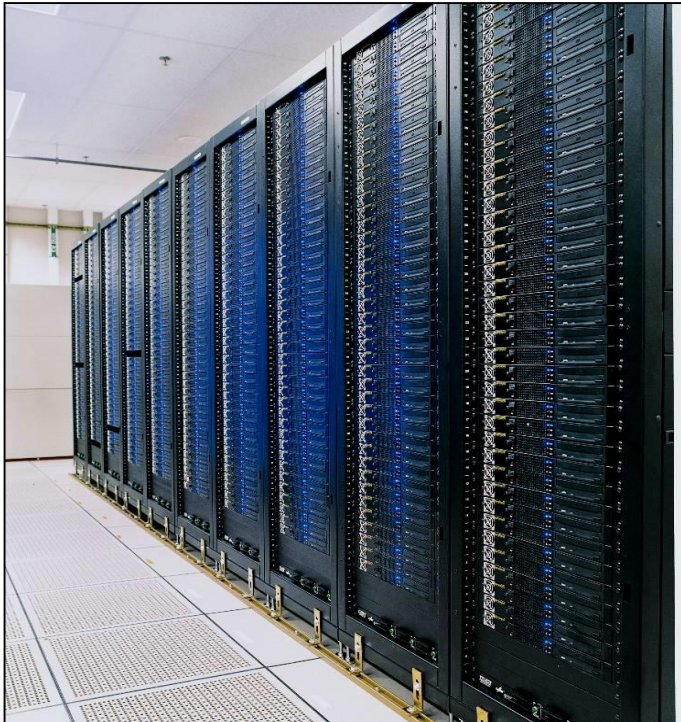


Full Hardware Utilization for Design Space Exploration



HPC: High Performance Computing

- HPC enables increased productivity and higher fidelity simulation - including more geometric detail and larger systems.
- HPC helps you make your product development process, more productive and efficient.
- Faster turnaround and larger models all mean better designs in less time.



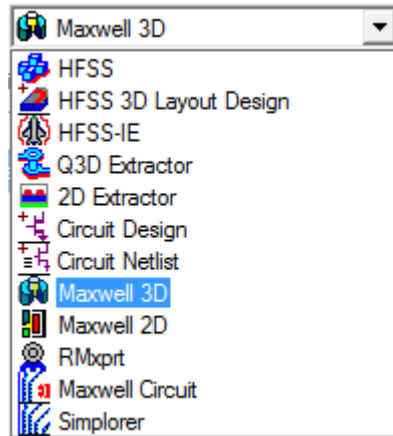
Faster

Bigger

Higher Fidelity

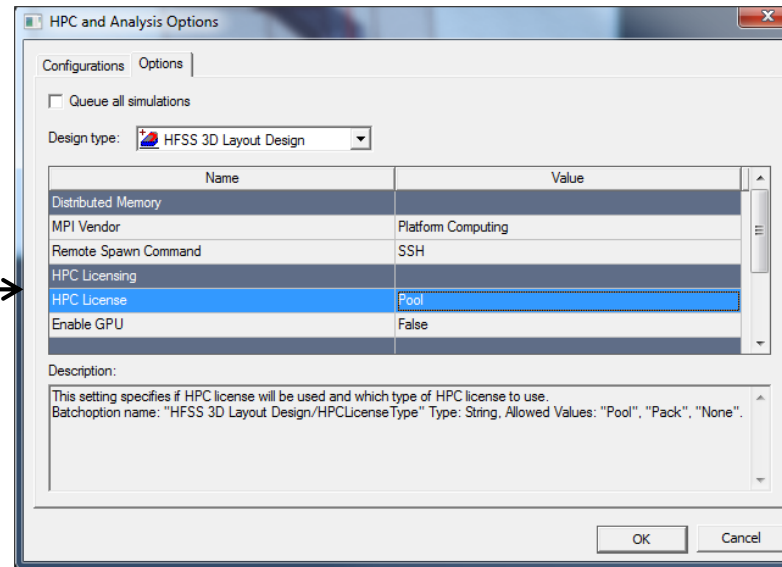
How to Enable HPC Pool License ?

- Tools > Options > HPC and Analysis Options
- Design Type:

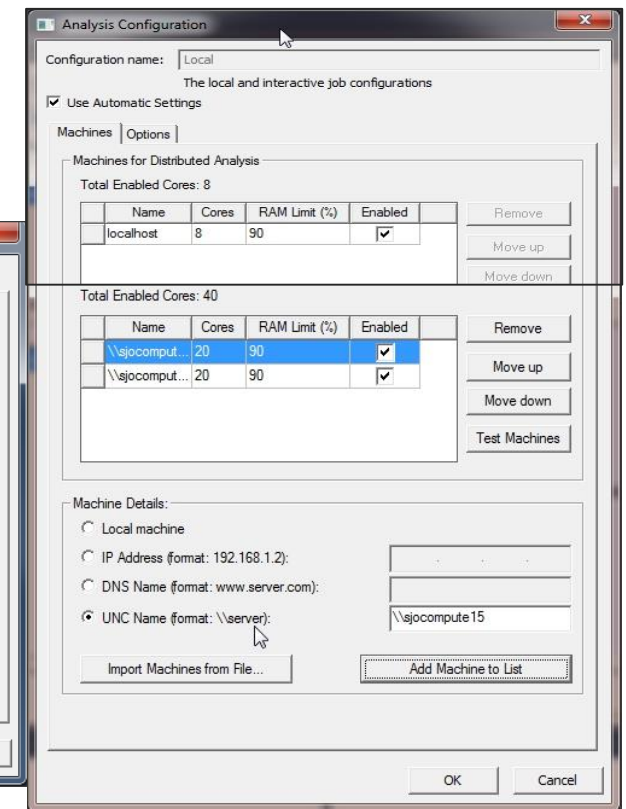


- Specify more than 1 cores
- Options Tab
 - HPC License - Pool

**Enable HPC
Pool**



HPC = Faster



Apple had 1536 tasks EM HPC workgroup license

DSO: Distributed Solve Option

**Distributed Solve
Option**



Design Space

Faster

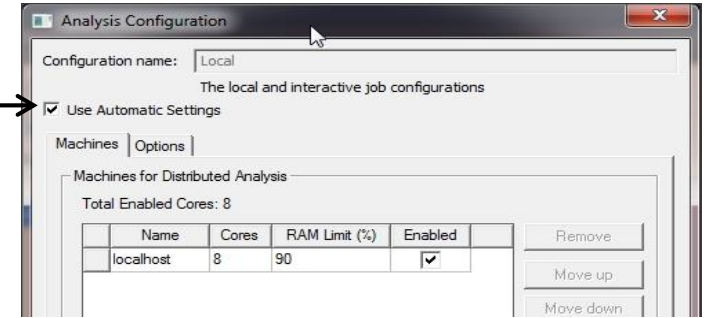
Distributed Solve Option

- Enables multiple *parametric variations* to be solved simultaneously on local and/or networked cores
- Each variable will utilize same HPC setting, which offers a near-linear speed-up with the number simultaneous variations (DSO tasks)
- Key for accelerating robust design (design of experiments, six sigma, etc.)

How to Enable DSO License ?

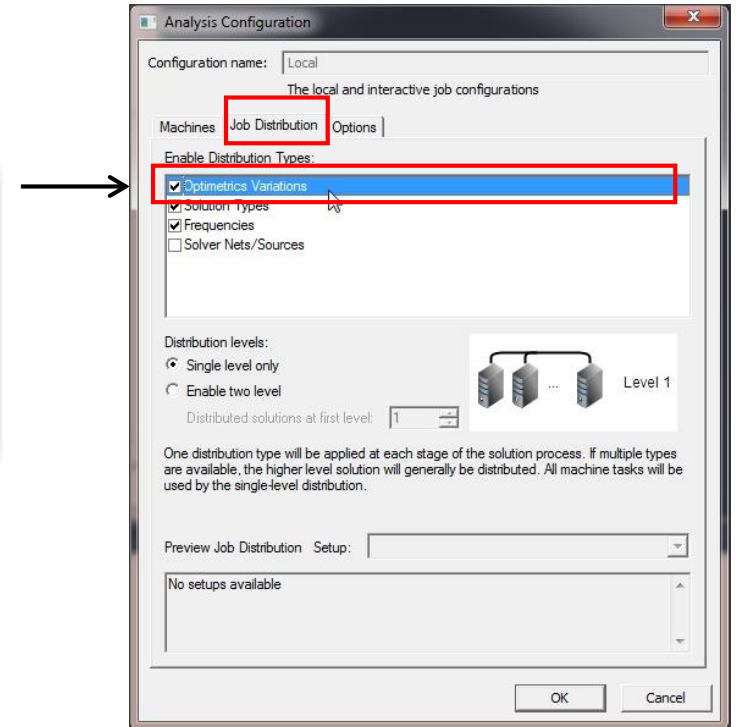
- Tools > Options > HPC and Analysis Options
 - HFSS, HFSS-IE and HFSS 3Dlayout:
 - DSO is enable if check ***Use automatic settings***

***HFSS, HFSS-IE,
HFSS3Dlayout
Enable DSO***



- Q2D/Q3D, Maxwell, Circuit and Simplorer:
 - In ***Job Distribution*** tab, checking ***Optimetrics Variations*** to enable DSO

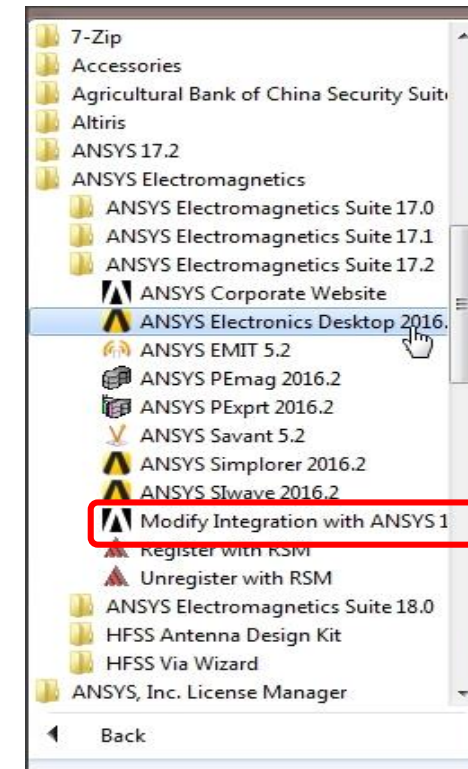
***Q2D/Q3D,
Maxwell,
Circuit,
Simplorer
Enable DSO***



Apple had 211 tasks DSO license

Software and License requirements

- **Software Requirements**
 - ANSYS Electronic Desktop 2016.2 (ANSYS EM Suite 17.2)
 - ANSYS Workbench 17.2 with Pre/Post
 - Integrated ANSYS Electronic Desktop with Workbench
- **License**
 - ANSYS HFSS with SI options
 - Optimetrics
 - HPC
 - DSO
 - ANSYS DesignXplorer



Conclusion

- **ANSYS provides unified platform for Signal Integrity Design Space Exploration, which covers pre-layout, post-layout simulation and manufacture tolerance study.**
- **DesignXplorer gives easy way to automatically set up SI for Design Space exploration and Optimization**
- **HPC and DSO will utilize all of the available hardware to accelerate simulation.**